OVERVIEW

We are a leading domestic platformized chip customization service provider in China, focusing on the research and development and commercialization of AI ASICs. Leveraging our independently developed IC technology platform and proprietary high-speed interface IPs, the AI ASICs that we customize address data transmission bottlenecks and achieve efficient interconnection of large-scale AI chip clusters, which aim to achieve full utilization of computing power in AI applications. We ranked third among domestic chip customization service providers in China in terms of AI ASIC revenue in 2025, and ranked second among domestic chip customization service providers in China in terms of chip design and delivery revenue in 2025, both according to CIC.

Our Chip Customization Services

Our chip customization services consist of chip design, chip delivery, and IP license. Chip design encompasses chip definition, front-end design, back-end design, tape-out, post-silicon support, and customer productization enablement. Chip delivery encompasses wafer-level silicon validation, advanced packaging and testing, and supply chain coordination.

A chip customization service mandate may begin with chip design, with or without IP license, and may be followed up chip delivery. Chip design and chip delivery represent our main sources of revenue, with combined revenue contribution of 83.9%, 73.3%, and 91.0% in 2023, 2024, and 2025, respectively.

The following table sets forth a breakdown of revenue by business line during the Track Record Period.

	For the Year Ended December 31,					
	2023		2024		2025	
	RMB	%	RMB	%	RMB	%
	(in thousands, except percentages)					
Chip Design	41,259	55.1	231,505	66.6	203,228	42.0
Chip Delivery	21,525	28.8	23,353	6.7	237,597	49.0
IP License	12,018	16.1	92,698	26.7	43,371	9.0
Total	**74,802**	**100.0**	**347,556**	**100.0**	**484,196**	**100.0**

Our revenue increased significantly from RMB74.8 million in 2023 to RMB347.6 million in 2024 and further by 39.3% to RMB484.2 million in 2025. However, revenue from each business line fluctuated during the Track Record Period, as affected by the service combination in, and the actual progress of, chip customization service mandates in any given year. From 2023 to 2024, both chip design revenue and IP license revenue increased significantly while chip delivery revenue increased by 8.5%, primarily due to multiple new projects completing the design stage and not yet reaching or completing the delivery stage in 2024. From 2024 to 2025, chip delivery revenue increased significantly and became the largest revenue contributor in 2025 while both chip design revenue and IP license revenue decreased, primarily due to multiple existing projects entering the delivery stage in 2025.

The following table sets forth a breakdown of revenue by service application type during the Track Record Period.

	For the Year Ended December 31,					
	2023		2024		2025	
	RMB	%	RMB	%	RMB	%
	(in thousands, except percentages)					
AI ASIC	38,658	51.7	314,932	90.6	437,262	90.3
Communication ASIC	35,421	47.4	32,624	9.4	46,934	9.7
Others	723	0.9	—	—	—	—
Total	74,802	100.0	347,556	100.0	484,196	100.0

Our AI ASIC revenue increased significantly from RMB38.7 million in 2023 to RMB314.9 million in 2024, and further increased by 38.8% to RMB437.3 million in 2025. Our AI ASIC revenue accounted for 51.7%, 90.6%, and 90.3% of our total revenue in 2023, 2024, and 2025, respectively. The increase in AI ASIC revenue both in an absolute amount and as a percentage of total revenue during the Track Record Period reflected our focus and commitment in AI ASIC customization services.

Our Platformized Model

We leverage our modular, intelligent, and automated IC technology platform to integrate our design capabilities and upstream and downstream resources to provide end-to-end chip customization services. We develop and license proprietary high-speed interface IPs, design and customize ASICs with advanced process nodes and 2.5D/3D packaging, and deliver chips through collaboration with third-party foundries and OSAT partners. Under this model, we lead the entire process from chip architecture design, logical design, design-for-test, and physical design to full lifecycle management, and efficiently coordinate with business partners in wafer fabrication and packaging testing, ensuring coverage of process nodes from 4 nm to 28 nm.

Our platformized model is defined by the following core attributes.

- ***IP Reuse and Efficiency:*** Through our modular IP library and mature design methodology, our chip customization services are provided with balanced design efficiency, quality consistency, and delivery speed.

- ***Seamless One-Stop Service:*** From architecture design to chip delivery, we minimize the burden and potential risks in multi-stage and multi-party collaboration to ensure project progress.

- ***Rapid Cross-Domain Expansion:*** Our platformized model supports technology migration across multiple fields such as AI and communications, helping customers explore new application scenarios.

- ***Experience-Based Know-How Accumulation:*** Notwithstanding continued process node iteration, our IC technology platform enables us to accumulate collective know-how and enrich our design toolchain, which in turn enhances our capabilities to identify and minimize project risks and hence increase project success rates.

OUR STRENGTHS

A leading domestic one-stop AI ASIC customization service provider in China, with advanced IC technology platform

We have independently developed an advanced IC technology platform that is modular, intelligent, and automated. Through deep integration of our proprietary IPs, intelligent toolchain, and standardized processes, we provide efficient one-stop chip customization services.

We strategically develop proprietary IPs in three areas: (i) high-speed data interface, (ii) high-speed memory interface, and (iii) chiplet interconnect interface. These proprietary high-speed interface IPs put us in an instrumental position in the AI development, where high-bandwidth, low-latency, and low-power interface IPs are highly required in light of the explosive growth in bandwidth and computing power demand. Our proprietary high-speed interface IPs thus form a significant puzzle for AI ASIC customization services.

We have independently developed two AI ASIC platforms, including one for cloud AI and one for edge AI, to address diverse customer needs. In addition, we have internal toolchain platforms, including one for front-end design tools and one for back-end design flow integration and delivery, to standardize research and development and delivery processes. Together, these platforms support our one-stop chip customization services throughout our design, verification, and delivery processes. They thus significantly improve design efficiency, optimize cost structure, mitigate chip customization project failure risk, and greatly shorten customers' time-to-market, thereby enhancing customers' competitiveness in their markets and their confidence in and loyalty to us.

Our IC technology platform modularizes and embeds our proprietary IPs and if necessary, third-party IPs throughout the entire AI ASIC customization lifecycle. Our platfomized model enables us to form a virtuous cycle where our proprietary IPs enhance our design efficiency while our design verification drives proprietary IP iterations. Real-world verification data in our ASIC customization continually drives the performance optimization and reliability enhancement of our proprietary IPs across different processes, accumulating a robust technology stack that covers architecture, verification, and PPA optimization. These scaled, continuously iterated, and real-world verified IP modules are transformed into stable technology outputs, forming the reusable core capabilities of our IC technology platform. This further empowers our continued advancement in chip customization services.

Independently developed proprietary high-speed interface IPs at the core of our IC technology platform

We highly value the strategic importance of independent development capabilities for proprietary high-speed interface IPs at the core of our IC technology platform. Our proprietary IP research and development system encompasses algorithm modeling, analog and digital circuit design, mixed-signal verification, layout implementation, and back-end integration. We integrate advanced process design capabilities with chiplet architecture iteration, systematically building a proprietary IP portfolio covering advanced process nodes from 4 nm to 12 nm, suitable for high-end applications such as AI, high-performance computing, and network communication.

Our proprietary high-speed interface IPs can support the current and next-generation high-performance computing.

High-Speed Data Interface IPs. They are empowered by the SerDes technology from 32 Gbps to 112 Gbps and support PCIe Gen5 and other advanced protocols. They are the cornerstones of building high-performance servers and high-end network devices, capable of handling massive data throughput and meeting the stringent requirements of cloud computing and large data centers.

High-Speed Memory Interface IPs. They support advanced standards such as HBM3 and LPDDR5x, and we have launched our LPDDR5x PHY IP based on 4-nm process node to the market for licensing. As the core memory solution for current AI chips and high-end GPUs, HBM3's high bandwidth and energy

efficiency currently represent a high level of memory interface, serving the top-tier AI and high-performance computing markets. LPDDR5x offers advantages such as high bandwidth, low power consumption, and high stability, effectively supporting the high-speed interaction of massive data during AI model training and inference, improving system computing efficiency and energy efficiency, and playing an irreplaceable role in fields such as AI, edge computing, and smart terminals.

Chiplet Interconnect Interface IPs. They provide 112 Gbps die-to-die high-speed extra-short-reach interconnect technology on a chiplet architecture and support advanced 2.5D/3D packaging. They break the physical limits of a single chip, allowing efficient integration of chiplets with different process nodes and functions, and form a key path to improving chip performance when traditional chip manufacturing has been approaching physical limits.

Currently, we are advancing the development of 112 Gbps long-reach SerDes based on the most advanced process nodes available domestically. This IP is a key technology for achieving AI chip interconnection and enabling efficient collaboration in clusters of thousands or even tens of thousands of computing cards. It is one of the most important cornerstones of our chip customization services.

We have deeply participated in the development of Chiplet Interconnect Interface Specification series, including five recommended national standards in China, which were officially implemented on March 1, 2026. As the first national standards in the field of chiplets, they mark a milestone breakthrough in the standardization of chiplets in China. Our participation in the development of these national standards underscores our technological strength and authority in defining industry norms in chiplet interconnect, reinforcing our leadership role in domestic high-end IPs.

By continuously strengthening the breadth and depth of our proprietary IPs and the flexibility of process adaptation, we not only effectively reduce the risk of external technology dependency but also build a multi-dimensional chip customization system encompassing design methodology, process collaboration optimization, and mass-production verification.

Leading complex chip design and advanced physical implementation technology capabilities, precisely matching the high-end market demand

Our chip customization capabilities range from chip system architecture definition to nanometer-level physical implementation, successfully overcoming the complexity challenges of ultra-large-scale integrated design and the physical size limitations of a single chip. High-end chips that we have customized cover core areas such as AI training and inference, high-speed storage, and network communications.

We are capable of complex chip design. We not only have mastered ultra-large-scale system-on-chip integration technology under advanced processes nodes such as 4 nm or 5 nm, but also focus on a chiplet heterogeneous integration architecture. Leveraging our proprietary 112 Gbps die-to-die interconnect technology, we break down a single large chip limited by photomask size into a high-performance heterogeneous integrated system with multiple chiplets working together. This architecture effectively addresses the urgent demand for unlimited computing power expansion in AI training chips. For example, our 4-nm AI server chip successfully delivered breaks through the traditional limitations of single-chip physical size and performance. Through our proprietary 112 Gbps ultra-high-speed interconnect technology and 2.5D advanced packaging design, we innovatively construct a high-bandwidth heterogeneous integrated system, achieving inter-chip connection speeds of up to 224 GB/s and computing power of over 160 TOPS. Meanwhile, the chip uses a RISC-V CPU as the management core to optimize power consumption, supports HBM3.0 high-bandwidth memory and 16 high-speed interfaces, with a memory access bandwidth of 819.2 GB/s, breaking the memory-wall bottleneck that restricts AI performance. While ensuring that signal transmission performance largely exceeds the industry standard, it achieves high energy efficiency and jitter-free stable operations at the scale of ten-thousand-card clusters, fully demonstrating our outstanding capability in delivering world-class complex large chips under advanced process technologies.

We also are capable of advanced physics implementation. We are one of the early movers to practice the concept of System-Technology Co-Optimization (STCO), breaking the traditional barriers between design, process, and packaging. Our focus extends beyond performance optimization at individual stage of the chip customization cycle to overall system optimization by introducing system-level requirements, process production capabilities, and packaging physical limits into joint iteration as early as the architecture definition stage. This helps us achieve optimal performance of our IPs and chip design, enabling us to precisely meet the strict demands of high-end markets for high bandwidth, low power consumption, fast time-to-market, and autonomy. This can eventually make us one of the few key strategic partners capable of delivering complex large chips and helping customers stand out in the computing power competition.

Strong business collaboration with global and domestic industry chains to build a stable delivery system

Amid intensified fluctuations in the semiconductor industry supply chain and the complex geopolitical environment, we have maintained a supply chain ecosystem that integrates world-class resources while being domestically independent and controllable. Through collaboration with global giants and leading domestic companies, we are establishing an industry-leading, stable delivery system, which not only ensures operating continuity but also provides customers with a full-cycle security barrier from design to delivery.

We have trustworthy collaborations with global semiconductor leaders. We have carried out the development and process adaptation verification of our key IPs for advanced process nodes to achieve accurate coupling of our IP performance and the process parameters of global giants. We thus have priority access to the state-of-the-art process node support of global giants and develop strong business relationship with them. At a time when advanced process capacity is in short supply globally, our priority access represents high recognition of our technical strength and business reputation in the industry, enabling us to provide customers with a stable supply with cutting-edge products with global competitiveness.

On the domestic supply chain front, we actively participate in the development of Foundation IPs for advanced processes nodes of mainstream domestic foundries. Through deep understanding of advanced processes, architectural design capabilities, experience in the development of Foundation IPs for mainstream domestic foundries, we are among the first domestically to master the design norms and characteristics of advanced process nodes, building exclusive collaborative barriers with leading foundries, forming a stable and sustainable technological cooperation ecosystem, and providing downstream customers with highly adaptable and highly reliable chip design support. Therefore, we are well positioned in the domestic advanced process ecosystem to help customer products achieve optimal PPA on domestic production lines and break the dependence of high-end chips on overseas supply chains.

In response to the stringent requirements of chiplets and high-performance computing for advanced packaging, we have signed a long-term strategic cooperation agreement with a leading domestic packaging and testing company. By securing its capacity of specialized advanced packaging production lines, we are breaking through the industry's capacity bottlenecks and contributing to the yield ramp-up and rapid mass production of complex large chips in high-density interconnect scenarios. This has enabled us to establish a deep collaboration mechanism and priority capacity assurance channel in packaging design, significantly enhancing the delivery certainty of complex large chips.

Based on our global-domestic dual layout, we have helped our customers build a resilient supply chain. We can flexibly allocate high-quality resources both internationally and domestically, providing customers with stable delivery services where advanced process nodes are accessible, core IPs are available, and high-end capacity is ensured. This makes us the preferred strategic partner for high-end customers seeking stable development in uncertain environments.

Experienced team with extensive industry background and an international perspective

Our core team is led by senior experts in the semiconductor industry, with an average of approximately 20 years of experience. They had been deeply involved in the full process of multiple international high-end chips from architecture definition and advanced process to packaging design and chip delivery. The team combines a global technological perspective with local industry experience, possessing solid engineering implementation capabilities in key areas such as AI ASICs, chiplet heterogeneous integration, and high-speed interface IPs. They are able to accurately assess technological trends, efficiently formulate research and development paths, and provide strong guidance for our strategic direction and technology roadmap.

Led by our core team, we have established a well-structured research and technical team. As of December 31, 2025, we had 317 research and technical staff, accounting for 81.7% of our total employees. Our research and technical staff covers chip architecture, IP development, physical implementation, packaging coordination, and mass production verification, forming a continuous iterative technology reserve and innovation capability. They are stationed in core domestic semiconductor industry regions in China such as Beijing, Shanghai, Nanjing, Suzhou, Wuxi, and Chengdu, supporting our sustainable development in the long run.

OUR STRATEGIES

Continue to expand our proprietary high-speed interface IP portfolio and strengthen the foundation of our IC technology platform

In light of the global computing power competition and the need for domestic independence and control, we will continue to invest in and develop proprietary high-speed interface IPs that are domestically independent and controllable, maintaining the advancement of our technology and strengthening the foundation of our IC technology platform. We will continue to focus on three key areas: (i) high-speed data interfaces such as 112 Gbps long-reach SerDes and 224 Gbps long-reach SerDes, (ii) high-speed memory interfaces such as HBM3e, LPDDR5x, and LPDDR6, and (iii) chiplet interconnect interfaces. We aim to build a more comprehensive enterprise IP library covering the entire chain of data transmission, data storage, and chiplet interconnect, providing core support for AI ASIC customization services.

Leveraging our 112 Gbps die-to-die interconnect technology and our leadership role in the national chiplet standardization, we are shifting our strategic focus towards a chiplet heterogeneous integration platform, transforming silicon-verified high-speed interface IP modules into standardized, reusable chiplet products, and enhancing compatibility with other interconnect standards such as UCIe.

We will further strengthen and iterate our cloud and edge AI ASIC platforms to enhance our chip customization capabilities to continually meet the rigorous customer demands. In addition, we will enrich our internal toolchain platforms, including the platform for front-end design tools and the platform for back-end design flow integration and delivery, to strengthen our standardized research and development and delivery processes.

Build an open and collaborative AI hardware ecosystem, creating a new benchmark for domestic AI ASICs

We plan to build an open and collaborative AI hardware ecosystem, aiming to become a benchmark enterprise in the field of domestic AI ASICs in China. In response to the diverse computing power demands for AI large model training and inference across cloud, edge, and terminal, we will not be limited to providing technical services only, but are committed to connecting core industry chain participants such as algorithm providers, system integrators, foundries and testing manufacturers, and end users in various vertical sectors. On one hand, we will leverage our one-stop advantages in proprietary high-speed interface IPs, advanced process ASIC customization, and 2.5D/3D packaging design to lower the development threshold and iteration cycle of high-performance AI ASICs, enabling customers to quickly realize

computing power deployment. On the other hand, we will work with upstream and downstream partners to jointly promote the formation of a complete localized supply chain for AI hardware systems, including edge AI servers, interconnect chiplets, and memory components.

Strengthen collaboration with foundry ecosystem and build a dual-track process collaboration system

We will continue with our asset-light strategy and establish collaboration with leading global foundries and domestic mainstream process platforms, focusing on the development of Foundation IPs and process collaboration optimization, integrating technological capabilities with production resources, providing customers with full-spectrum capacity assurance covering advanced to mature process nodes, and significantly enhancing project delivery certainty and supply chain resilience.

On the global side, we will consolidate our existing business relationships with leading global foundries. By participating in early design technology co-optimization for advanced process nodes such as 3 nm or 2 nm, we have priority access to design rules, model libraries, and capacity support for the latest process nodes, ensuring that our proprietary IPs and ASIC customizations meet the highest international performance standards and satisfy high-end customers' pursuit of optimal PPA. On the domestic side, we will participate in the ecological co-construction of domestic advanced process lines, carrying out Foundation IP verification, process characteristic modeling, and yield improvement initiatives, promoting the influence and application of domestic process nodes in the high-end chip field.

Carry out strategic global layout and build an open and inclusive IC ecosystem

We will implement a global development strategy, aiming to become an IC technology platform with international influence.

We will actively expand our global marketing and service network, integrate into domestic and global mainstream semiconductor supply chains, and promote our one-stop services to globally influential cloud service providers, system manufacturers, and AI enterprises, achieving diverse expansion of our market footprint. In addition, we will leverage a global perspective to establish research and development centers or liaison offices in semiconductor innovation hubs in the world, extensively attract system architects and engineering experts with cutting-edge experience, and build a diverse and complementary team of top-notch talent to ensure continued technological leadership.

We will prudently seize strategic merger and acquisition opportunities to optimize resource allocation. Although we primarily develop through organic growth, we will flexibly evaluate and selectively acquire high-quality targets that are complementary to our business, such as those with complementary IP technologies, specific domain design capabilities, or key customer channels, to rapidly complete the technology puzzle or accelerate regional market penetration. Specifically, we may consider potential targets that specialize in IP research and development in the IC industry based on the following general selection criteria: (i) the business of the target should exhibit synergies with or complement to our business; (ii) the management team or research and development team of the target should possess relevant industry knowledge, extensive experience, and strong innovative capability in the industry; (iii) the target should not be involved in major legal disputes or compliance issues; and (iv) the target should possess clearly defined intellectual property rights to avoid potential patent disputes. According to CIC, as of December 31, 2025, there are over 50 available targets that meet our selection criteria in the market. As of the Latest Practicable Date, we had not identified any specific acquisition targets and were not in ongoing negotiations with any specific acquisition targets.

OUR CHIP CUSTOMIZATION SERVICES

Chip Design

The chip design covers chip definition, front-end design, back-end design, tape-out, post silicon support, and customer productization enablement.

The following diagram sets forth the key stages of chip design.

CHIP DESIGN STAGES

- ***Chip Definition***. We collaborate with customers to define chip requirements, specifications, and architecture, and provide IP selection and integration solutions to lay the foundation for subsequent design.

- ***Front-End Design***. We translate the defined architecture into register transfer level code, RTL code, conduct design verification, and develop prototypes and firmware to validate the correctness and feasibility of the chip design.

- ***Back-End Design***. We convert the verified RTL code and design for testability structure into a physical layout through synthesis, physical implementation, and package design, ensuring manufacturability. Our physical implementation workflow includes placement, clock tree synthesis, routing, timing sign-off, and power analysis.

- ***Tape-Out***. We deliver the files of GDSII to the foundry for chip tape-out, where photomasks are produced for wafer manufacturing. Prior to production, we conduct an e-job review (a layer-by-layer verification of photomask correctness) to validate manufacturing and design compliance.

- ***Post Silicon Support***. We drive continued yield improvement, optimize test programs, and implement strict quality control throughout the manufacturing lifecycle.

- ***Customer Productization Enablement***. We collaborate with customers to carry out systematic test, application debugging, and compliance test.

Chip Delivery

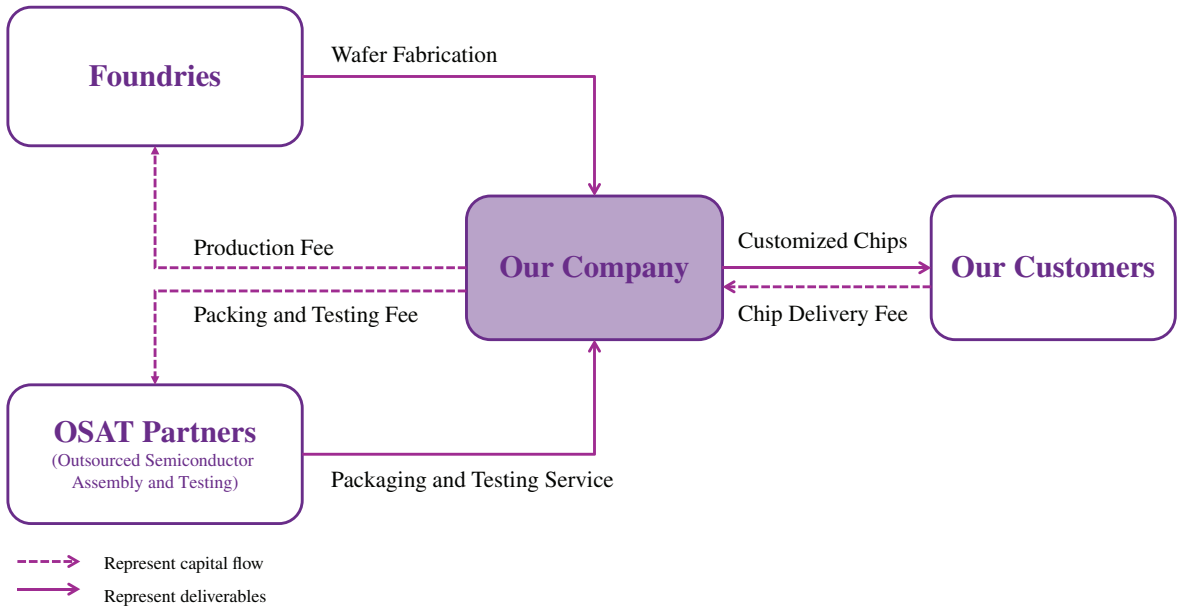
To better serve our customers, reduce their development costs, and improve efficiency, we also offer end-to-end chip delivery based on our customers' demands. Our chip delivery process includes the following key stages:

- ***Wafer-Level Silicon Validation***. We perform comprehensive silicon validation, including performance and reliability testing on silicon.

- ***Advanced Packaging and Testing***. We offer advanced packaging solutions, which encompass a diverse range of technologies, including flip chip, system-in-package, multi-chip modules, and 2.5D/3D packaging. We also perform final testing to ensure the quality, performance, and reliability of the packaged chips before delivery.

- ***Supply Chain Coordination***. We coordinate closely with third-party foundries and outsourced semiconductor assembly and test partners, which we refer to as OSAT partners, to ensure the stable mass production of chips. Through integrated management of the entire supply chain, we deliver qualified chip products to customers. This involves establishment of collaborative cooperation mechanisms, production planning and forecasting, order placement, inventory management, and professional logistics arrangement, including transportation, customs clearance, and label design.

The following diagram illustrates our chip delivery model and relationships with key stakeholders.



During the third-party foundries production execution, we coordinate with the relevant service providers on technical specifications, production schedules, and quality requirements, and participate in key stages such as quality control and yield improvement. Ownership of certain proprietary IPs embodied in the designs remains with us. Our payments to foundries and OSAT partners are generally made on a wafer-based and volume-based pricing basis, and our settlement terms are typically subject to milestones, delivery, and agreed credit terms as set out in the agreements. We generally do not make upfront payments to secure capacity, except where commercially necessary.

We collaborate closely with our customers throughout the product development and commercialization process. Depending on the specific engagement, our deliverables typically include customized AI ASICs with technical documentations. We work with customers at various stages, from product definition and specification alignment to design-in support and performance optimization, to ensure that our designs are effectively integrated into their end products. Through this collaborative approach, we aim to provide customers with high-performance, power-efficient, and cost-optimized chips that shorten their development cycles, enhance product competitiveness, and improve overall system performance.

IP License

Our chip customization services are driven predominantly by in-house, independently developed proprietary IPs, supplemented by a selectively chosen portfolio of third-party IPs. Our proprietary IPs currently center on chip interfaces, featuring a full-spectrum suite of AI chip interfaces, which serves as a cornerstone for the further advancement of AI. Upon completion of research and development, verification, and production validation, we license our proprietary IPs to our customers for use in their own chip development projects. Some of the IPs are also used in our chip customization services. Our deliverables generally include the licensed IP, related technical documentation, integration and implementation guidelines, and ongoing technical support.

In addition, we have participated in the development of foundry Foundation IPs for domestically advanced process nodes, fostering a robust ecosystem that drives the maturation of local process technologies.

Pricing

Chip Design

Chip design is priced on a project-by-project basis through arm's length negotiations with our customers, taking into account factors such as technical specifications, customization requirements, project cycles, and project non-recurring engineering work, and is agreed with our customers in statement of works and contracts. The payment terms are generally structured on a milestone basis, with payments linked to the achievement of agreed development stages as stipulated in the orders or agreements.

Chip Delivery

The pricing factors of our chip delivery include process node, wafer costs, packaging non-recurring engineering work and costs, supporting non-recurring engineering work, and volume. Test fixture costs — covering items such as probe cards, load boards, and sockets — are also factored into our pricing, along with the associated test costs. The total fees that we charge will be determined based on the tiered price per chip and the volume delivered. We may also offer volume discounts or long-term supply arrangements to certain customers, where commercially appropriate.

IP License

IP license is charged as (i) IP license fees or (ii) royalties for chip delivery of chips incorporating our IPs. IP license fees are priced on a project-by-project basis through arm's length negotiations with our customers, taking into account factors such as technical specifications and performance requirements of the IPs, the extent of customization, expected delivery volume, prevailing market rates, competitive landscape, and the long-term potential of customer relationship. Our royalty is typically structured as a usage-based revenue sharing arrangement, calculated as a percentage of the average sale price or on a fixed price per unit basis for chips incorporating our IPs, and payable upon customers' commercial production and sales. As a result, our royalties are closely linked to customers' shipment volume, enabling recurring and scalable revenue. The payments for the IP license fees are generally structured as either a full upfront payment or a combination of an upfront payment and subsequent milestone-based payments. The payments for royalties are periodically charged, as stipulated in agreements.

Project Backlog and Execution Performance

The following table sets forth our project backlog movement in terms of contract value during the Track Record Period.

	For the Year Ended December 31,		
	2023	2024	2025
	(RMB in thousands)		
Opening balance of contract value (excluding VAT) at the beginning of the year	130,909	454,344	486,827
Add: Contract value (excluding VAT) secured during the year	398,237	380,039	492,886
Less: Revenue recognized during the year	74,802	347,556	484,196
Closing balance of contract value (excluding VAT) at the end of the year	**454,344**	**486,827**	**495,517**

The following table sets forth our project backlog movement in terms of contract number during the Track Record Period.

	For the Year Ended December 31,		
	2023	2024	2025
Projects brought forward from the previous year	22	26	18
Add: Number of new projects secured during the year	45	31	64
Less: Number of projects completed during the year	41	39	55
Projects carried forward to the following year	**26**	**18**	**27**

The year-on-year increase in the closing balance of contract value at the end of the year from 2023 to 2025 was primarily due to an increase in the volume of signed contracts driven by the continued business growth.

During the Track Record Period, there were nil, 2, and 8 loss-making projects in 2023, 2024, and 2025, respectively. We incurred losses from these projects primarily due to our strategy to secure strategic customers and foster long-term cooperation. Majority of the customers of the loss-making projects during the Track Record Period subsequently entered into new contracts with us. The total losses resulting from these projects were nil, RMB0.1 million, and RMB6.6 million in 2023, 2024, and 2025, respectively. The revenue and gross loss attributable to loss-making projects during the Track Record Period were generally insignificant relative to our total revenue and gross profit. Therefore, the occurrence of these loss-making projects did not have a material adverse effect on our overall business operations.

APPLICATION TYPE

AI ASICs

We strategically specialize in the end-to-end, customized design of AI ASICs. We provide advanced AI ASIC customization services to customers primarily operating in data centers, edge computing servers, automotives, mobile devices and other related industries.

The following table sets forth major AI ASIC categories that our chip customization services cover.

Category	Key Features	Major Application Scenarios
Cloud AI ASICs	• Ultra-high compute density • Massive bandwidth • Low-latency interconnects	• Data centers • Large-scale AI model training and inference • High-performance computing clusters
Edge AI ASICs	• Balanced high performance with moderate power consumption • Real-time processing • Support for 5G infrastructure and industrial AI workloads	• Industrial AI systems • Edge computing gateways and servers
Terminal AI ASICs	• Ultra-low power • High integration • Compact form factor • Optimized for mobile or embedded devices and on-device AI inference	• Automotives • Mobile or embedded devices • Intelligent terminals • On-device AI inference in consumer and IoT products

Communication ASICs and Others

We also provide chip customization services for communication ASICs and other applications, including communication and wireless ASICs and data center networking and interconnect ASICs.

The following table sets forth communication ASICs and other chip categories that our chip customization services cover.

Category	Key Features	Major Application Scenarios
Communication and Wireless ASICs	• High-speed data transmission and signal processing • Process in wireless connectivity applications • Support for 5G and next-generation wireless communication standards • Integrate multiple communication protocols and interface IPs • Optimized for low latency, power efficiency and signal integrity	• 5G infrastructure and wireless communication systems • Networking and telecom equipment • Wireless modules and connectivity systems
Data Center Networking and Interconnect ASICs	• Facilitate high-speed data transmission • High-bandwidth, low-latency data switching and interconnect capabilities • Support for high-speed interface standards and chip-to-chip interconnect • Scalable architecture for data center and cloud infrastructure • Optimized for reliability and power efficiency	• Data center and cloud computing infrastructure • High-speed networking and switching systems • High-performance interconnect fabrics

OUR PROPRIETARY IP PORTFOLIO

We have developed strong capabilities in high-speed data transmission and memory interface technologies, which are critical for AI and high-performance computing chips. Our technologies enable chips to transfer large amounts of data quickly and reliably, both between chips and between processors and memory. This helps address one of the biggest performance bottlenecks in AI systems — data bandwidth and latency.

Our proprietary IP portfolio includes high-speed data interface IPs, high-speed memory interface IPs, and chiplet interconnect IPs, primarily serving the growing performance needs of AI-related applications.

- ***High-Speed Data Interface IPs***. Our high-speed data interface IPs enable fast and reliable data transmission between chips and external systems. These solutions support advanced computing and AI applications by providing stable, high-bandwidth connectivity across complex hardware environments.

- ***High-Speed Memory Interface IPs***. Our high-speed memory interface IPs enable processors and computing chips to communicate efficiently with memory modules. These solutions support high data throughput and low latency, which are essential for AI and high-performance computing workloads.

- ***Chiplet Interconnect IPs***. We also develop chiplet interconnect IPs used in advanced packaging and chiplet architectures. These solutions enable efficient data exchange within AI accelerators and high-performance computing systems while maintaining strong energy efficiency and reliability.

The following table sets forth our core proprietary IP portfolio.

Category	Key Strengths	Features	Major Application Scenarios
High-Speed Data Interface IP: 32G MP SerDes and PCIe Gen5	• Multi-protocol support at data rates of 1 to 32 Gbps, with integrated protocol subsystems and burst-mode clock and data recovery for passive optical network applications • Fully in-house IP design with proprietary integration and customization capabilities • Advanced phase-locked loop and high-performance receiver architecture for low power consumption, small area and high performance • Comprehensive support covering integration, packaging, power and signal integrity at chip and system levels, and thermal co-design	• Modular architecture with multiple data lanes, a common lane and a synthesized lane • Advanced architecture with low power consumption, compact area and high performance, supporting multiple protocol standards • Flexible clocking scheme with multi-level phase-locked loops, enabling configurable data rates and multi-channel aggregation and bifurcation • High protocol flexibility for applications across interconnect, storage and communication standards	• PCIe 5.0 applications, including AI server, networking, switch, retimer, passive optical network, and field programmable gate array, etc.
High-Speed Data Interface IP: 112G LR SerDes and PCIe Gen6	• Multi-protocol support at data rates of 1 to 112 Gbps, including Ethernet and PCI Express, with integrated protocol subsystems for rapid system-on-chip integration • Fully in-house IP design with proprietary integration and customization capabilities • Advanced digital signal processing architecture with adaptive algorithms for low power consumption, compact area and high performance • Comprehensive support covering integration, packaging, power and signal integrity at chip and system levels, and thermal co-design	• Modular architecture with eight data lanes, a common lane and a synthesized lane • High-performance digital signal processing architecture for robust signal recovery in complex channel conditions • Compliance with latest industry standards for seamless ecosystem compatibility	• AI training and inference ASICs • High-performance computing and data center infrastructure • Networking equipment, smart network interface cards, and acceleration cards • Network switches and routers • Desktops, workstations, and servers

Category	Key Strengths	Features	Major Application Scenarios
High-Speed Memory Interface IP: LPDDR5x	• Full-stack, fully in-house development from circuit to system architecture, with deep node- and application-level optimization • Superior signal integrity with low-jitter clocking architecture and robust timing closure under process, voltage, and temperature variations	• Modularity and high adaptability: on-demand assembly supported by diversified input or output slices • Custom analog clock tree design with low skew and strong noise immunity	• AI training and inference ASICs • High-end smartphones • Advanced driver-assistance systems
High-Speed Memory Interface IP: HBM3/3E	• Comprehensive physical layer functions, including initialization, delay calibration, voltage and temperature compensation, impedance calibration, configuration, and status registers, built-in self-test, and interface with memory controllers • Support for JEDEC-compliant high bandwidth memory generation 3 and generation 3 extended memory, with data rates of up to 9,600 megabits per second, compatible with 2.5D packaging	• Optimized for high performance, low latency, small area, low power consumption, and ease of integration, delivered as a hard macro with flexible controller configurations • Integrated input and output and phase-locked loop modules, enabling flexible configurations and compatibility with a wide range of memory devices	• High-performance AI training and inference ASICs • Graphics processing • Networking equipment
High-Speed Memory Interface IP: ONFI 5.1.	• Ultra-efficient power, performance and area optimization • Reduced silicon area with high-density modular architecture and minimized clock tree footprint • Low latency enabled by optimized buffer chain and streamlined clock path design, meeting stringent ONFI timing requirements	• Modular and reusable architecture with flexible scalability through decoupled design • Comprehensive ONFI power management with support for retention mode and sleep mode • Fine-grained clock gating for optimized balance between performance and power consumption	• Enterprise solid-state drives • AI solid-state drives • Mobile and automotive applications

Category	Key Strengths	Features	Major Application Scenarios
Chiplet Interconnect IP: 112G XSR/XSR+ D2D/C2C	• Short-reach die-to-die and chip-to-chip interconnect, 1 to 112 gigabits per second, controller and physical layer subsystem • Fully in-house design, complete ownership of core integration, customizable tuning, and analysis for 2.5D/3D packaging • All-analog architecture, low power, small silicon area, high performance • Comprehensive support for integration, packaging, power integrity and signal integrity, thermal co-design, and technical services	• Flexible layout, separate transmit, and receive hard macros, each with eight data lanes, one common lane, and one synthesis lane • Ultra-low power with high-performance analog design at high data rates	• High-performance computing and AI ASICs • Workstations and server ASICs • Die-to-die and chip-to-chip interconnect

OUR TECHNOLOGIES

Reusable AI ASIC Design and Engineering Capabilities

We have established comprehensive and reusable AI ASIC design and engineering capabilities to support efficient, high-quality, and rapid development of customized AI ASICs.

We have developed two core proprietary AI ASICs platforms to address diverse customer needs: the edge AI ASIC platform and the cloud AI ASIC platform. Our proprietary AI ASIC platforms feature highly modular architectures, building full-stack capabilities spanning core computing power, subsystem integration, and system-level assembly, laying a solid foundation for efficient ASIC development and rapid delivery.

Throughout the design and verification processes, we emphasize the development of in-house automation tools and flows to improve efficiency, quality, consistency, and cost-effectiveness, while shortening development cycles. These tools include the SoC toolkit for automated design, memory subsystem generation tool, automated design flow management tool, and intelligent verification tool.

Leveraging the proprietary customized design flow integration and delivery platform, we have established a standardized research and development and delivery system covering the entire chip lifecycle. This platform enables end-to-end automated management from synthesis, DFT, physical implementation, to sign-off.

Advanced 2.5D/3D and Heterogeneous Integration Technologies

We are building advanced 2.5D/3D and heterogeneous integration technologies to support next-generation chip architectures.

Our 2.5D/3D design methodology is characterized by cross-disciplinary integration, which demands comprehensive capabilities spanning both chip design and packaging design. Different from the traditional separation of chip design and packaging links, our methodology embeds the collaborative optimization logic of chip architecture and packaging scheme into the early stage of chip definition. Rooted in our technical platform, which has precipitated standardized, scalable design methodologies through numerous high-end chip projects, this platform-integrated methodology enables a holistic consideration of chip functional requirements, performance indicators, packaging forms, supporting the formulation of optimal 2.5D/3D integration solutions for diverse scenarios. Leveraging this cross-disciplinary integrated design methodology, it effectively improves chip integration density, reduces signal delay and power consumption, and fully meets the high-performance and high-reliability demands of AI, high-performance computing, and other cutting-edge fields.

To further enhance the competitiveness of our 2.5D/3D and heterogeneous integration technologies, we have independently developed 3D DRAM controller IP. As the core bridge connecting logic chips and 3D DRAM memory, our proprietary 3D DRAM controller IP is specifically optimized for 2.5D/3D stacking scenarios, enabling efficient data transmission and management between logic units and 3D DRAM memory. By enhancing 3D-DRAM bandwidth utilization efficiency, the controller delivers highly efficient data supply, supporting efficient training and inference of trillion-parameter AI models.

RESEARCH AND DEVELOPMENT

Our deep passion for innovation, coupled with our strong research and development capabilities have allowed us to enjoy a significant technological edge. We believe that our commitment to research and development is the cornerstone of our growth strategy and a key driver of our competitive advantage. Our technologies are at the forefront of innovation, specializing in cutting-edge research and development of advanced technologies. As of December 31, 2025, we had 7 research and development centers in major cities in China.

Our Capability

Since our inception, our substantial investment in research and development has fueled our rapid growth by enabling us to continually enhance our solution portfolio and advance our technological capabilities, including recruiting, training, and retaining high-caliber technology talents with rich experience.

As of December 31, 2025, we had 317 research and technical staff, accounting for 81.7% of our total employees. Our research and technical team supports our research and development initiatives and undertakes design work for our design projects, where needed. Our core development personnel possess extensive experience in the design of high-performance chips, enabling us to enhance existing performance, diversify our offering portfolio, and strengthen our innovation-driven competitiveness in this industry.

We have been committed to investing in our research and development talents and initiatives. We incurred research and development expenses of RMB90.9 million, RMB175.5 million, and RMB239.0 million in 2023, 2024, and 2025, respectively.

Our Structure

We have established three core research and development divisions, including front-end design, back-end design, and IP development. The front-end and back-end design divisions are primarily responsible for the research and development of our proprietary AI ASIC platforms and design methodologies, including the independent research and development of internal design and verification tools, design flows, in-house tools and delivery systems. The IP development division focuses on the complete closed-loop operation for our proprietary IPs, encompassing research, development, and commercialization support.

We retain key management and technical staff with competitive remuneration packages and welfare benefits. We also invest in training programs to upskill our key staff. In addition, we recruit candidates with relevant knowledge and skills by hiring headhunting companies and campus recruitment.

Research and Development Process

We identify potential research and development projects based on our development strategy, industry trends, and customer needs. We have established a comprehensive process to ensure strict control and oversight of our research and development activities. Our research and development process may vary from 90 days to 540 days, depending mainly on the technological complexity and customers' requirements.

Our research and development process is systematically divided into the following stages.

- ***Project Initiation and Pre-Research Phase***. This stage involves feasibility analysis, execution planning, and design or verification plan formulation and review, laying a foundation to avoid risks, align with needs, and ensure investment effectiveness.

- ***Design and Development Phase***. Our research and technical team conducts integrated design, development, simulation, and verification in line with standardized processes and quality controls, reducing defects, improving efficiency, and promoting technical reuse.

- ***Validation Phase***. For proprietary IP development projects that require test chip tape-out, GDS II files are sent to the foundry, followed by silicon validation after wafer return. For other projects, design and simulation results are verified.

- ***Project Closure Phase***. After final acceptance, the project is closed with a summary of cost, technical outcomes, and key learnings, facilitating experience precipitation and research and development process optimization.

INTELLECTUAL PROPERTY

We regard our trademarks, patents, domain names, know-how, trade secrets, and similar intellectual property as critical to our success. As of the Latest Practicable Date, we had 88 granted patents, all of which are invention-related patents in China. As of the Latest Practicable Date, we had 50 IC layout design registrations, 49 copyrights, nine registered trademarks, and one domain name in China.

We acquire patents through self-development. As of the Latest Practicable Date, we owned all of our patents as well as patent applications. During the Track Record Period and up to the Latest Practicable Date, we did not experience any threatened or pending disputes relating to infringement of intellectual property rights that would have a material adverse effect on our business.

We rely on a combination of copyright, patent, and trademark law, trade secret protection, confidentiality agreements with employees, and intellectual property, and confidentiality provisions in our agreements with third-party suppliers to protect our intellectual property rights. We have established a range of internal control policies and measures to ensure our ability to protect our intellectual property rights and operate without infringing, misappropriating, or otherwise violating the valid, enforceable intellectual property rights of third parties. However, we cannot assure you that we will prevail on patent infringement claims against third parties. See "Risk Factors — Risks Relating to Our Business and Industry — We may not be able to sufficiently protect or enforce our intellectual property rights, patent rights, or trade secrets across the world, and our efforts to do so may be costly."

For more details of our material intellectual property, see "Statutory and General Information — B. Further Information About Our Business — 2. Our Material Intellectual Property Rights" in Appendix VI to this document.

SALES AND MARKETING

Sales Team and Strategy

Our marketing department is responsible for enhancing our brand awareness and promoting our new and existing offerings, aiming to expand our popularity, influence, coverage, and penetration. As of December 31, 2025, our sales and marketing team consisted of 24 members. Our sales team has an extensive presence across China, with dedicated project practice managers based in Shanghai overseeing the full lifecycle of each project with professional end-to-end support.

Our sales and marketing strategy aims to strengthen brand leadership, expand market reach, and enhance customer relationships through a multi-dimensional sales network, proactive customer engagement, and integrated marketing initiatives.

We primarily adopt a direct sales model. We focus on developing long-cycle relationships with major customers, supported by strong customer stickiness and recurring orders.

Marketing and Brand Building Efforts

We are committed to establishing Joinsilicon as a recognized brand associated with innovation and quality. Our marketing and branding efforts include:

- ***High-Quality Delivery and Service Reputation***. Our focus on providing high-quality chip design and IPs and strong post-sales services is central to our business growth and customer engagements. Our post-sales services for ASIC design services generally includes post-silicon issue debugging, yield improvement support, test program optimization, and technical support. Our post-sales services for IP license business generally includes technical documentation, technical support, integration and implementation guideline, training, and IP maintenance and

updates. Our dedicated service team ensures close collaboration and clear communication throughout the entire process. This commitment to reliability and responsiveness has built deep customer trust, which is reflected in our strong retention rate and has solidified our reputation as a trusted partner.

- ***Multi-Channel Brand Communication***. We strive to expand our market share through enhancing our brand influence through an integrated communication approach that leverages online platforms, sector-leading media, and participation in industry events.

- ***Strengthen Global Presence and Market Recognition***. Moving forward, we will continue to deepen our presence and strengthen our market position in China, while actively pursuing global expansion and broadening our international business footprint, through expanded sales channels, strategic partnerships and customer engagement, and international marketing efforts. These efforts have significantly enhanced our visibility and brand recognition in the global IC design market.

OUR CUSTOMERS

During the Track Record Period, our customers primarily consisted of chip and system providers in AI, communications, and other industries. In 2023, 2024, and 2025, revenue generated from our top five customers in each applicable year accounted for 74.4%, 95.1%, and 78.3% of our total revenue, respectively, and revenue generated from our largest customer in each applicable year accounted for 32.2%, 81.5%, and 37.4% of our total revenue, respectively.

The following table sets forth certain information regarding our top five customers during the Track Record Period.

Customer	Transaction Amount	Percentage of Total Revenue	Year of Commencement of Business Relationship	Customer Background	Purchase	Credit Terms	Payment Methods
	(RMB in thousands)	*(%)*					
For the Year Ended December 31, 2023							
Customer A	24,073	32.2	2022	A non-listed company located in China and mainly engaged in provision of high-end communication chip	Chip Design and Chip Delivery	Prepayment or 30 days upon the invoice	Bank wire transfer
Customer B	9,679	12.9	2022	A non-listed company located in China and mainly engaged in provision of edge AI chip	Chip Design and IP License	Prepayment	Bank wire transfer
Customer C	8,333	11.1	2022	A non-listed company located in China and mainly engaged in provision of sensor chip	Chip Design and Chip Delivery	Prepayment	Bank wire transfer
Customer D	7,641	10.2	2021	A non-listed company located in China and mainly engaged in provision of network security chip	Chip Delivery	10 to 30 days upon the invoice	Bank wire transfer
Customer E	5,979	8.0	2021	A non-listed company located in China and mainly engaged in provision of high-performance computing chip	Chip Delivery and IP License	Prepayment or 30 days upon the invoice	Bank wire transfer
Total	**55,705**	**74.4**					

Customer	Transaction Amount	Percentage of Total Revenue	Year of Commencement of Business Relationship	Customer Background	Purchase	Credit Terms	Payment Methods
	(RMB in thousands)	*(%)*					
For the Year Ended December 31, 2024							
Customer B	283,256	81.5	2022	A non-listed company located in China and mainly engaged in provision of edge AI chip	Chip Design, Chip Delivery, and IP License	30 days upon the invoice	Bank wire transfer
Customer F	17,537	5.0	2022	A non-listed company located in China and mainly engaged in provision of CPU	Chip Design and Chip Delivery	10 days upon the invoice	Bank wire transfer
Customer G	13,351	3.8	2022	A non-listed company located in China and mainly engaged in provision of AI-DPU	Chip Design and Chip Delivery	Prepayment	Bank wire transfer
Customer H	10,018	2.9	2024	A company located in China and mainly engaged in provision of automotive electronics, listed on Hong Kong Stock Exchange	Chip Delivery	Prepayment	Bank wire transfer
Customer I	6,689	1.9	2024	A non-listed company located in China and mainly engaged in provision of communication chip	Chip Design	30 days upon the invoice	Bank wire transfer
Total	**330,851**	**95.1**					

Customer	Transaction Amount	Percentage of Total Revenue	Year of Commencement of Business Relationship	Customer Background	Purchase	Credit Terms	Payment Methods
	(RMB in thousands)	*(%)*					
For the Year Ended December 31, 2025							
Customer B	181,240	37.4	2022	A non-listed company located in China and mainly engaged in provision of edge AI chip	Chip Design, Chip Delivery, and IP License	30 days upon the invoice	Bank wire transfer
Customer H	114,807	23.7	2024	A company located in China and mainly engaged in provision of automotive electronics, listed on Hong Kong Stock Exchange	Chip Delivery	Prepayment	Bank wire transfer
Customer J	34,653	7.2	2024	A non-listed company located in China and mainly engaged in provision of server	IP License	Prepayment	Bank wire transfer
Customer K	25,915	5.4	2023	A non-listed company located in China and mainly engaged in provision of display chip	Chip Design and IP License	Prepayment or 30 days upon the invoice	Bank wire transfer
Customer L	22,381	4.6	2025	A non-listed company located in China and mainly engaged in provision of chip solutions	Chip Design	Prepayment	Bank wire transfer
Total	**378,996**	**78.3**					

The following sets forth the salient terms of the contracts with our customers for our chip design.

- ***Specification.*** The agreement defines specific design services, deliverables, and project timeline.

- ***Payment.*** Customers typically make payments on a milestone basis. Non-recurring engineering fees are generally non-refundable. If the customer cancels the project, it is liable for all costs incurred up to the cancellation date, including third-party expenses and internal labor cost. Additional fees may apply for project delays caused by the customer.

- ***Delivery and Acceptance.*** Technical deliverables are submitted together with an acceptance form. The customer generally has five business days to review and sign the form or raise objections.

- ***Intellectual Property***. In a spec-in model, subsystems independently developed by us are retained by us, while the integrated ASIC design belongs to the customer. In a netlist-in model, design methodologies belong to us, and the customer obtains an exclusive right to use them for the specific project.

- ***Warranty***. We warrant that the services do not infringe third-party IP. If a third-party claim arises solely from our services, we will pay resulting damages subject to certain conditions.

- ***Termination***. The agreements can be terminated by mutual consent.

The following sets forth salient terms of the contracts with our customers for our chip delivery.

- ***Specification***. The agreement defines the scope of our chip delivery and packaging and testing services.

- ***Payment***. We generally require full prepayment before we place orders with foundries and assembly and test plants.

- ***Customer Obligations***. Customers are obliged to complete payments according to the contract terms and provide estimated mass production volumes.

- ***Delivery***. We arrange shipment and maintain insurance during transit. Title and risk of loss pass to the customer upon signed acknowledgment of receipt at the designated delivery location.

- ***Confidentiality***. We must maintain confidentiality of the technical information provided by the customer and shall not disclose it to third parties without prior approval.

- ***Termination***. The agreements can be terminated by mutual consent.

The following sets forth salient terms of the contracts with our customers for our IP license.

- ***Payment***. We typically charge IP license fees either in full upfront or through a combination of an upfront payment and milestone-based payments.

- ***Specification***. The agreement defines the scope of the licensed IP and any related technical services to be provided.

- ***Limitation***. Customers may only use our technologies within the agreed scope and manner as set out in the contract and are not permitted to use them beyond such scope.

- ***Delivery and Acceptance***. We deliver our IP modules in accordance with the agreed conditions, timeline, and delivery method set out in the contracts. Upon delivery, customers are generally granted an inspection period of 5 days to review the technical specifications and confirm acceptance.

- ***Supporting***. We generally provide technical support free of charge for a period of 12 months following delivery, after which annual service fees may be charged in accordance with the rates agreed in the contracts.

- ***Duration***. The term of our IP license agreements is generally determined by the lifecycle of the chips that incorporate our licensed IPs.

- ***Intellectual Property***. We retain all intellectual property rights in our technologies, and customers are granted limited usage rights under the contracts.

- ***Confidentiality***. The parties agree not to disclose any confidential information relating to the contracts or technologies licensed to any third party without prior written consent.

- ***Termination***. Our IP license agreements may be terminated by mutual consent or upon the occurrence of a material breach, bankruptcy, or liquidation of the other party.

Revenue generated from our top five customers accounted for 74.4%, 95.1%, and 78.3% of our total revenue in 2023, 2024, and 2025, respectively. We expect to continue to experience revenue concentration for the foreseeable future.

The concentration of revenue contribution from our major customers is primarily due to the nature of our business model, under which we typically serve a relatively limited number of customers, each with a material contract value and a comparatively long project cycle.

Despite the revenue concentration from our top five customers during each period of the Track Record Period, our Directors are of the view that we are not subject to any material risks of customer reliance and our business is sustainable based on the following:

(i) According to CIC, customer concentration is common among those chip customization service companies with a high revenue contribution from AI-related applications, as the relevant customer base is relatively concentrated and primarily consists of a limited number of large downstream AI cloud service providers;

(ii) Except for Customer A in 2023, Customer B in 2024, and Customer B and Customer H in 2025, none of our top five customers in any period of the Track Record Period individually contributed over 15% of our total revenue for the same period;

(iii) We have maintained stable relationship with all of our top five customers during the Track Record Period since we established business relationship with them. Certain key customers, such as Customer B, have signed recurring contracts with us during the Track Record Period;

(iv) Customer B mainly provides edge AI chips. We commenced business relationship with it since 2022 and provided one-stop services that cover IP license, chip design, and chip delivery to it. Revenue from Customer B accounted for 81.5% of our total revenue in 2024, because we completed chip design for various contracts with it and recognized revenue accordingly during the year. However, revenue contribution from Customer B subsequently decreased to 37.4% in 2025. As a result, our revenue concentration with Customer B decreased during the Track Record Period; and

(v) We have been actively expanding our customer base and successfully secured new major customers such as Customer H, Customer J, and Customer L during the Track Record Period. We believe that it is mutually beneficial and complementary for our major customers to maintain business relationship with us. Our proprietary high-speed interface IPs, advanced IC technology platform and technologies, strong execution capabilities, and proven track record of customer satisfaction have strengthened our customers' confidence in and loyalty to us, as demonstrated by the continued expansion of our customer base during the Track Record Period.

All of our top five customers in each period during the Track Record Period were Independent Third Parties. As of the Latest Practicable Date, none of our Directors, their close associates, or any Shareholders that, to the best knowledge of our Directors, owned more than 5% of our issued share capital as of the Latest Practicable Date, had any interest in any of our top five customers in each period during the Track Record Period.

During the Track Record Period and up to the Latest Practicable Date, we did not have any material disputes with, nor did we receive any material complaints from, our customers. In addition, there were no material breaches of agreements during the Track Record Period and up to the Latest Practicable Date.

OUR SUPPLIERS

During the Track Record Period, our suppliers primarily include providers of (i) tape-out services and wafers, (ii) third-party IPs, and (iii) semiconductor packaging materials.

Our procurement team formulates procurement plans based on anticipated sales, manufacturing lead times, and production schedules. In accordance with such plans, we place purchase orders with our foundry suppliers, who manufacture wafers based on our IC designs, and engage packaging and testing partners to complete chip packaging and testing.

We select our suppliers based on evaluation criteria including pricing, product quality, technical capability, and delivery performance, and maintain an approved supplier list to ensure consistent standards and supply stability. We primarily manage the quality of products and services provided by our suppliers through regular performance evaluations, quality inspections, and contractual quality assurance requirements.

In 2023, 2024, and 2025, purchases from our top five suppliers in each applicable year accounted for 65.2%, 85.7%, and 65.1% of our total purchases, respectively, and purchases from our largest supplier in each applicable year accounted for 28.1%, 48.7%, and 22.9% of our total purchases, respectively. During the Track Record Period, our procurement was sourced primarily from suppliers in China and South Korea.

The following table sets forth certain information regarding our top five suppliers during the Track Record Period.

Supplier	Transaction Amount	Percentage of Total Purchase	Year of Commencement of Business Relationship	Supplier Background	Product or Service Purchased	Credit Terms	Payment Methods
	(RMB in thousands)	*(%)*					
For the Year Ended December 31, 2023							
Supplier Group A . .	30,153	28.1	2021	A multinational group mainly engaged in provision of chip solutions, listed on Nasdaq Stock Market	Raw materials and IP	Prepayment	Bank wire transfer
Supplier Group B . .	23,450	21.8	2023	A multinational group mainly engaged in provision of EDA and IP, listed on Nasdaq Stock Market	IP	Prepayment	Bank wire transfer
Supplier C	6,368	5.9	2023	A non-listed company located in China and mainly engaged in provision of chip design services	Chip design services	Prepayment or 30 days upon the invoice	Bank wire transfer
Supplier D	5,555	5.2	2021	A company located in China and operated as an agent of semiconductor foundry, listed on Nasdaq Stock Market	Raw materials	Prepayment	Bank wire transfer
Supplier E	4,490	4.2	2023	A company located in China and mainly engaged in chip solutions, listed on Shanghai Stock Exchange	Chip design services	Prepayment	Bank wire transfer
Total	**70,016**	**65.2**					

Supplier	Transaction Amount	Percentage of Total Purchase	Year of Commencement of Business Relationship	Supplier Background	Product or Service Purchased	Credit Terms	Payment Methods
	(RMB in thousands)	*(%)*					
For the Year Ended December 31, 2024							
Supplier F	107,672	48.7	2023	A multinational company mainly engaged in semiconductor manufacturing, listed on Korea Exchange	Raw materials	Prepayment or 60 days upon the invoice	Bank wire transfer
Supplier G	50,924	23.0	2024	A non-listed company located in China and mainly engaged in provision of electronic component services	Raw materials	Prepayment	Bank wire transfer
Supplier Group A . .	14,517	6.6	2021	A multinational group mainly engaged in provision of chip solutions, listed on Nasdaq Stock Market	Raw materials	Prepayment or 30 days upon the invoice	Bank wire transfer
Supplier Group H .	8,869	4.0	2024	A group located in China and mainly engaged in semiconductor manufacturing, listed on Shanghai Stock Exchange	Raw materials	Prepayment	Bank wire transfer
Supplier I	7,499	3.4	2024	A non-listed company located in China and mainly engaged in provision of electronic component services	Raw materials	Prepayment	Bank wire transfer
Total	**189,481**	**85.7**					

Supplier	Transaction Amount	Percentage of Total Purchase	Year of Commencement of Business Relationship	Supplier Background	Product or Service Purchased	Credit Terms	Payment Methods
	(RMB in thousands)	*(%)*					
For the Year Ended December 31, 2025							
Supplier G	47,399	22.9	2024	A non-listed company located in China and mainly engaged in provision of electronic component services	Raw materials	Prepayment	Bank wire transfer
Supplier J	28,858	13.9	2024	A non-listed company located in China and operated as an agent of semiconductor foundry	Raw materials	Prepayment or 60 days upon the invoice	Bank wire transfer
Supplier K	23,000	11.1	2025	A company located in Japan and mainly engaged in provision of electronic component services, listed on Tokyo Stock Exchange	Raw materials	Prepayment	Bank wire transfer
Supplier Group H .	21,406	10.3	2024	A group located in China and mainly engaged in semiconductor manufacturing, listed on Shanghai Stock Exchange	Raw materials	Prepayment	Bank wire transfer
Supplier L	14,274	6.9	2024	A non-listed company located in China and mainly engaged in provision of semiconductor solutions	Raw materials	Prepayment	Bank wire transfer
Total	**134,937**	**65.1**					

The following sets forth the salient terms of our purchase agreements with our suppliers.

- ***Term and Termination***. We generally have a term of three years for our suppliers subject to renewal by mutual agreement. We have right to terminate the agreement with immediate effect in the case of the termination conditions stipulated in the agreement by providing written notice.

- ***Price.*** For some suppliers with established long-term relationships, the framework agreement does not specify quantities or prices. Specific quantities and prices are detailed in separate purchase orders.

- ***Principal Obligations.*** Suppliers are responsible for timely delivery to our designated location, bearing all freight and insurance costs, and must meet quality standards. We generally have seven days upon receipt to inspect for defects. Title and risk of loss transfer only upon our signed acceptance.

- ***Payment Terms.*** Our suppliers operate on either a prepayment or postpaid basis. For postpaid orders, we typically settle the relevant amounts within 30 to 60 working days after acceptance and invoice receipt.

- ***Warranty.*** We typically stipulate a one-year warranty period commencing from the date of acceptance.

All of our top five suppliers in each period during the Track Record Period were Independent Third Parties. As of the Latest Practicable Date, none of our Directors, their close associates, or any Shareholders that, to the best knowledge of our Directors, owned more than 5% of our issued share capital as of the Latest Practicable Date, had any interest in any of our top five suppliers in each year during the Track Record Period.

During the Track Record Period and up to the Latest Practicable Date, we did not experience quality issues with, or breaches of agreements by, our suppliers that materially affect our operations, nor did we encounter any material disruptions in our service offerings due to shortages of supply. During the Track Record Period, we did not experience any material fluctuations in the prices of our raw materials.

Overlapping of Customers and Major Suppliers

To our best knowledge, Supplier C, one of our top five suppliers in 2023, is the wholly-owned subsidiary of Customer E, one of our top five customers in 2023. In 2023, 2024, and 2025, our revenue generated from Customer E amounted to RMB6.0 million, nil, and nil, respectively, accounting for 8.0%, nil, and nil of our total revenue for the same period. In 2023, 2024, and 2025, our purchases from Supplier C amounted to RMB6.4 million, RMB4.7 million, and nil, respectively, accounting for 5.9%, 2.1%, and nil of our total purchase for the same period. We provided tape-out and IP license services to Customer E in 2023. In 2023 and 2024, we outsourced certain non-core research and development workflows of our proprietary IPs to Supplier C due to manpower constraints. According to CIC, the overlapping of customers and suppliers is not uncommon in the chip customization industry, because semiconductor companies often take on different roles at different stages of the value chain under the industry's specialized division of labor and collaborative development model. Our sales to Customer E and purchases from Supplier C were conducted on individual basis and were not conditional on each other. Transactions with Customer E and Supplier C were conducted in the ordinary course of business, under normal commercial terms, and on an arm's length basis.

During the Track Record Period, Supplier I, one of our top five suppliers in 2024, was also our customer in 2025. In 2023, 2024, and 2025, our purchases from Supplier I amounted to nil, RMB7.5 million, and nil, respectively, accounting for nil, 3.4%, and nil of our total purchases for the same period. In 2023, 2024, and 2025, our revenue generated from Supplier I was nil, nil, and RMB14.3 million, respectively, accounting for nil, nil, and 2.9% of our total revenue for the same period. In 2024, we

purchased certain electronic components from Supplier I and other suppliers for our project needs and built up additional inventory. In 2025, as we had overstocked these electronic components, we sold part of these inventory to Supplier I at its request. The overlap in our business relationship with Supplier I was one-off in nature, and we do not expect such overlap to recur.

QUALITY CONTROL

Service Quality and Safety

We have established a rigorous and well-structured quality management system that integrates industry-leading standards and best practices to ensure reliability and customer satisfaction. Our overall quality framework is built upon ISO 9001 quality management system. In addition, in the area of functional safety, we have implemented a Road Vehicles Functional Safety system and obtained ISO 26262 ASIL-D certification.

From design to production, quality is embedded throughout our entire service lifecycle. We employ rigorous validation and verification processes to ensure reliability and compliance with industry standards, with all research and development workflows and project documentation managed through an IT-backed system for consistency and traceability. We actively promote quality awareness through comprehensive training programs on quality systems and tools, and KPI-driven assessments. Our continued improvement initiatives encourage proactive participation, rewarding teams for contributions to process optimization and innovation.

In addition, we work closely with customers to ensure compliance with their specific product development, manufacturing, and shipping requirements while conducting thorough contract reviews to align expectations. Our customer feedback mechanisms allow us to promptly address concerns and drive continued improvement.

During the Track Record Period and up to the Latest Practicable Date, we did not experience any material disputes regarding our service quality.

INFORMATION SECURITY AND DATA PRIVACY

In the course of our business operations, we collect and store internal data primarily relating to finance, operations, research and development, and transaction data with business partners. Such data is mostly managed through digital IT systems except for a small portion of data that is stored on local computers or in the form of physical documents. Given that we only conduct transactions with enterprises, our business generally does not involve the collection or processing of customers' personal information.

All of our IT servers are housed in our own data center with controlled access and automated environmental monitoring. Access to systems is managed through a centralized IAM (identity and access management) platform that governs user authentication and authorization based on their roles and is subject to internal audit reviews. Employees are required to sign confidentiality agreements upon joining and receive training on data protection protocols, with access rights deactivated upon departure. For document management, we have established a confidential document platform where documents are categorized into four levels, namely internal, confidential, highly confidential, and top secret, with access strictly restricted according to the confidentiality level.

Our operating environment and research and development environment are physically isolated. Sensitive and research-and-development-related data is stored in dedicated physical storage devices within isolated environments, with clear access controls over data access. The transfer of sensitive data shall be subject to step-by-step approval by responsible persons at all levels in accordance with its confidentiality level. Upon approval, the data transmission shall be executed by the IT department through relevant systems. No other personnel shall be authorized to perform data transmission.

To reinforce our data security and protection measures, we have implemented a comprehensive approach that includes secure data storage protocols and strict transmission policies to ensure the confidentiality and integrity of sensitive information. Moreover, we have implemented a robust information backup management system, which sets forth the guiding principles, detailed procedures, and mechanisms for data recovery. In addition, we have formulated an information security management scheme to set out the general guidance and principles of our information security management, under which we have established a series of policies and procedures, including inter alia, policies on system operation management, password management, corporate trade secret protection, and procedures on document control and confidentiality management. These systems, policies, and procedures collectively form a solid framework that safeguards our data and upholds our stringent standards for information security.

During the Track Record Period, we did not engage in any cross-border data transmissions. In the course of our business operations, we may share our own business-related data with third parties strictly on a need-to-know basis, in accordance with applicable laws and relevant contractual arrangements. During the Track Record Period and up to the Latest Practicable Date, as advised by our PRC Legal Advisor, we have not been subject to any material claim, penalty, or incident in relation to data privacy and security, and our Directors are of the view that we have complied with PRC data privacy and protection laws and regulations in all material respects.

EMPLOYEES

As of December 31, 2025, we had 388 full-time employees. The majority of our employees were based in China during the Track Record Period and up to the Latest Practicable Date.

The following table sets forth a breakdown of our full-time employees by functional departments as of December 31, 2025.

	As of December 31, 2025	
Function	Number of Employees	Percentage of Total Employees
Research and technical	317	81.7%
Management and general administration	47	12.1%
Sales and marketing	24	6.2%
Total	**388**	**100.0%**

We believe the strength and talent of our workforce are critical to the success of our businesses, and we continually strive to attract, develop, and retain personnel commensurate with the needs of our businesses. We always strive to provide employees with comprehensive social benefits, a wide range of career growth opportunities, and a diverse work environment. Furthermore, we are committed to providing a safe and healthy workplace, which is backed by strict policies, robust training, and safety recognition awards. We are committed to the recruitment, education, development and advancement of our personnel. Additionally, we place special emphasis on the building of a talent pipeline and cohesive company culture. We have established a comprehensive system for employee training and development, covering topics such as professional competencies, corporate culture and values, workplace ethics, compliance awareness and others.

We recruit our employees based on a range of factors such as their industry experience in the IC design industry, their educational background, and our vacancy needs. We primarily recruit employees through social recruitment, supplemented by campus recruitment to build a balanced talent pipeline.

As required by laws and regulations in China, we participate in various employee social security plans that are organized by municipal and provincial governments, including, among other things, pension, medical insurance, unemployment insurance, maternity insurance, work-related injury insurance, and housing fund plans through a PRC government-mandated benefit contribution plan. Specifically, we are

required under PRC law to make contributions from time to time to employee benefit plans for our China-based employees at specified percentages of the salaries, bonuses, and certain allowances of such employees, up to a maximum amount specified by the local governments in China.

We are committed to establishing competitive and fair remuneration. In order to effectively motivate our staff, we continually refine our remuneration and incentive policies. We conduct performance evaluations for our employees regularly to provide feedback on their performance. Compensation for our staff typically consists of base salary, performance-based bonus, and share-based incentives.

We typically enter into standard employment agreements, confidentiality agreements, and non-compete agreements with our senior management and core employees. These contracts include a standard non-compete covenant that prohibits the employee from competing with us, directly or indirectly, during his or her employment and for a certain period of time thereafter. We maintain a good working relationship with our employees, and we have not experienced any material labor disputes.

PROPERTIES

As of the Latest Practicable Date, we do not own any land use rights or properties in China. As of the Latest Practicable Date, we operated our businesses primarily through 11 leased properties for office purposes in China, with a total gross floor area of over 8,000 square meters.

As of December 31, 2025, none of the properties leased by us had a carrying amount of 15% or more of our consolidated total assets. According to Chapter 5 of the Listing Rules and section 6(2) of the Companies Ordinance (Exemption of Companies and Prospectuses from Compliance with Provisions) Notice, this document is exempted from the requirements of section 342(1)(b) of the Companies (Winding Up and Miscellaneous Provisions) Ordinance to include all interests in land or buildings in a valuation report as described under paragraph 34(2) of the Third Schedule to the Companies (Winding up and Miscellaneous Provisions) Ordinance.

Filing of Lease Agreement

During the Track Record Period and up to the Latest Practicable Date, despite our efforts, we were unable to complete lease registrations for nine leased properties used as offices, primarily because the landlords had not obtained the ownership certificates or individual landlords were unwilling to cooperate in filing the lease registrations. Under PRC laws and regulations, we may be required to file with the relevant government authority executed leases. As advised by our PRC Legal Advisor, the failure to file the lease agreements for our leased properties will not affect the validity of these lease agreements, but the competent housing authorities may order us to file the lease agreements in a prescribed period of time and impose a fine ranging from RMB1,000 to RMB10,000 for each non-filed lease if we fail to complete the registration within the prescribed timeframe. The aggregate maximum penalty for the non-compliance relating to the filing of lease agreements would be RMB90,000 based on agreements in force as of the Latest Practicable Date. During the Track Record Period and up to the Latest Practicable Date, we had not received any notice from any regulatory authority relating to administrative penalties or enforcement actions arising from these non-registered leases. If we were ordered to make such payment, we will do so promptly and within the prescribed time period. Therefore, our Directors are of the view that these non-registrations would not have a material adverse effect on our business, financial condition, or results of operations. Going forward, we intend to take into consideration the lessors' title and willingness to provide assistance in registering lease agreements when renewing existing leases or entering into new leases.

INSURANCE

We consider our insurance coverage to be adequate and in accordance with the commercial practices in the industries in which we operate. Our employee-related insurance consists of statutory social insurance contributions, including pension insurance, maternity insurance, unemployment insurance, work-related injury insurance and medical insurance. In addition, we provide comprehensive supplementary commercial insurance for our full-time employees covering accidental death or disability, critical illness, and outpatient and inpatient medical expenses. We also extend medical insurance coverage

to our employees' eligible dependents. Furthermore, we maintain third-party insurance policies during transit covering certain potential risks and liabilities, such as product liability. Our management will evaluate the adequacy of our insurance coverage from time to time and purchase additional insurance policies as needed.

ENVIRONMENTAL, SOCIAL, AND GOVERNANCE

We recognize that environmental, social and governance (ESG) factors are key to assessing sustainable development and long-term value creation. To strengthen our management capabilities, we have formulated the Environmental, Social and Governance (ESG) Management Measures (《環境、社會及管治(ESG)管理辦法》) and established an ESG governance structure in which the Board of Directors provides oversight and decision-making, while the ESG working group is responsible for management and execution, ensuring the effective implementation of ESG practices.

The Board of Directors, as the highest decision-making body for ESG matters, reviews our ESG strategy, objectives, key risks and opportunities, evaluates annual plans and performance, and provides support in budgeting, policies and resource allocation. To implement the Board of Directors' decisions, we have established an ESG working group responsible for daily ESG management, including promoting energy-saving and environmental practices, managing ESG data collection and reporting, and coordinating across departments to integrate ESG requirements into daily operations.

Environmental Protection

We regard environmental protection as a fundamental cornerstone of our sustainable development and strictly comply with the Environmental Protection Law of the People's Republic of China (《中華人民共和國環境保護法》) and other applicable laws and regulations. As our principal business focuses on chip customization and related technical services and does not involve energy-intensive processes such as wafer fabrication, our operations do not generate material industrial emissions including wastewater, waste gas or solid waste. Nevertheless, we continue to improve our internal environmental management system, focusing on energy use and office waste management at our office and research and development premises to enhance resource efficiency and reduce environmental impact from daily operations.

Resource Management

Energy management has been incorporated as a key focus of our daily operations. Through energy consumption monitoring, energy-saving measures and enhanced employee awareness, we aim to improve energy efficiency. Electricity represents our largest source of energy consumption. As our business grows, strengthening resource conservation and utilization efficiency remains essential to enhancing operational resilience and sustainability. Accordingly, we implement governance targets and energy-saving and carbon reduction initiatives to further optimize energy use. The table below sets forth our electricity consumption during the Track Record Period:

	For the year ended December 31,		
	2023	2024	2025
Energy Consumption			
Electricity Consumption (MWh)	458.9	910.0	1,365.9
Energy Consumption Intensity (MWh/million RMB revenue)	6.1	2.6	2.8

To improve the efficient use of energy, we have set the following management objectives based on our business characteristics and will continue to track progress each year:

- Electricity intensity is expected to decrease by 5.0% by 2030.

At present, we primarily adopt the following measures to improve resource utilization efficiency:

- Switching off air-conditioning and other electricity-consuming equipment in office areas when not in use;
- Turning off lighting and other non-essential electronic equipment during non-working hours, with periodic inspections by administrative staff to prevent unnecessary electricity consumption.

Emissions Management

Non-hazardous waste management

Our non-hazardous waste mainly consists of paper generated from daily office activities. During the Track Record Period, total non-hazardous waste increased in line with business expansion, while emission intensity declined. This was mainly due to (i) the adoption of paperless systems and digital collaboration platforms, which reduced paper consumption at the source, and (ii) improved paper classification and recycling practices, enhancing resource utilization efficiency. The table below sets forth our non-hazardous waste emissions and emission intensity during the Track Record Period:

	For the year ended December 31,		
	2023	2024	2025
Total Non-Hazardous Waste (Tons)	0.3	0.5	0.7
Non-Hazardous Waste Intensity (Tons/million RMB revenue)	0.004	0.002	0.001

Addressing Climate Change

Identification and management of climate-related risks

Climate change is an increasing challenge for global economic and industrial development. We actively respond to the PRC's "carbon peaking and carbon neutrality" strategy and global climate initiatives by integrating low-carbon principles into our management and operations. Through energy-saving measures, green office practices and supply chain carbon reduction initiatives, we enhance our climate resilience and green competitiveness.

Climate-related issues have been incorporated into our environmental and risk management framework. We regularly assess the potential impacts of climate change on our operations and develop response measures for both physical and transition risks. Examples of identified risks, opportunities, potential impacts and corresponding measures are set out below:

Risk/Opportunity Type	Description	Potential Impact	Measures
Physical Risks			
Extreme weather risks	• Extreme weather events induced by climate change, such as heavy rainfall, typhoons, and cold waves	• Disruptions to the operation of office and research and development premises	• Strengthen disaster prevention measures at office and research and development premises and improve emergency response plans and drills

Risk/Opportunity Type	Description	Potential Impact	Measures
Transformation Risks			
Technical risks	• The industry is evolving toward lower power consumption, higher energy efficiency and the adoption of green materials	• Lagging technology roadmaps may lead to a decline in competitiveness	• Invest in key technologies to develop low-power, high-efficiency products and collaborate with upstream and downstream partners to promote a green supply chain
Policy risks	• Strengthening of policies and regulations (including requirements on energy efficiency, carbon emissions and recycling)	• Rising compliance costs and heightened disclosure and customer requirements	• Monitor regulatory and customer requirements, strengthen internal policies and compliance training, and establish standardized data and disclosure processes
Opportunities			
Market expansion	• Driven by the "carbon peaking and carbon neutrality" targets, downstream industries are accelerating their green transition	• Opportunities from green supply chain access, enhanced ESG reputation attracting customers and talent, and policy support and incentives	• Capture these opportunities by strengthening carbon data management, customer communication and ESG disclosure

Greenhouse gas management

In accordance with applicable greenhouse gas accounting standards and guidelines, we are progressively establishing a greenhouse gas inventory and management framework and improving mechanisms for data collection, calculation, verification and record keeping. Our operational emissions primarily arise from purchased electricity consumed at our office and research and development premises. Building on our existing data foundation and disclosure strategy, we are gradually expanding data collection and disclosure for other indirect emissions, including business travel and employee commuting. We will continue to monitor climate-related performance indicators and further reduce operational carbon emission intensity through low-carbon practices and the exploration of green energy applications. The table below sets forth our Scope 2 and Scope 3 greenhouse gas emissions and emission intensity during the Track Record Period:

	For the year ended December 31,		
Greenhouse Gas Emission	2023	2024	2025
Scope 2: Direct GHG Emissions (tCO2e)	321.2	637.0	956.1
GHG Emission Intensity (Scope 2) (tCO2e/million RMB revenue)	4.3	1.8	2.0
Scope 3: Indirect GHG Emissions (tCO2e)	78.5	136.2	103.8
GHG Emission Intensity (Scope 3) (tCO2e/million RMB revenue)	1.0	0.4	0.2

To mitigate greenhouse gas emissions, we have set the following management objectives based on our business characteristics, taking into account changes in business scale, adjustments in office and research and development space, evolution in workforce structure, and the utilization of green electricity, and will continue to track progress each year:

- GHG emission intensity is expected to decrease by 5.0% by 2030.

At present, we primarily adopt the following measures to reduce our emission intensity:

- Integrating energy-saving practices into daily operations, including requiring lights and air-conditioning systems to be switched off when not in use, thereby reducing Scope 2 greenhouse gas emissions;

- Utilizing digital collaboration platforms and cloud-based conferencing systems to replace non-essential cross-regional business travel, significantly reducing Scope 3 emissions from transportation;

- Promoting low-carbon commuting practices by encouraging employees to use public transportation, thereby reducing the carbon footprint associated with daily commuting.

Social Responsibility

Employment and Labor Standards

We regard our employees as key assets and are committed to providing a fair, diverse and safe working environment with opportunities for development. We continuously enhance our human resources management system and follow principles of equality, diversity and non-discrimination in recruitment. All employees enter into labor contracts in accordance with applicable laws and are provided with benefits such as commercial insurance, welfare leave, welfare points and annual health examinations. We have established safety and emergency management systems for our office and research and development premises and conduct regular safety training and drills. In addition, employee grievance and feedback channels are in place with strict confidentiality and fair handling procedures to safeguard employees' rights. We also provide a structured training system covering onboarding, professional development and annual training, including corporate policies and culture, professional skills, compliance, information security and emergency management.

Intellectual Property Management

We attach great importance to the protection of intellectual property rights and trade secrets and strictly comply with applicable laws and regulations, including the Patent Law of the People's Republic of China (《中華人民共和國專利法》). Intellectual property protection is incorporated into our corporate governance and risk management framework. We have implemented internal policies such as the Trade Secret Management System of Joinsilicon Microelectronics (《中茵微電子商業秘密管理制度》) and the Intellectual Property Management System (《知識產權管理制度》) to safeguard our R&D achievements and core technologies. Through procedures covering research and development results registration, patent applications, rights protection and trade secret management, we ensure timely and effective protection of technological innovations. We also conduct regular IP compliance reviews and strengthen employees' awareness through training, while respecting others' intellectual property and safeguarding the security and independence of our technological assets.

Customer Service Management

We place great importance on building long-term partnerships with our customers and continuously improve our customer service and technical support systems. We regularly conduct technical exchanges with customers and align our services and technology roadmap with their product plans, upgrade needs and industry trends to meet evolving requirements. Through structured research and development processes and rigorous project management, we enhance service efficiency and quality management. We have also

established a technical support and customer feedback mechanism to promptly address technical and quality issues and improve customer satisfaction. Going forward, we will continue to strengthen our service capabilities and provide reliable and efficient technical support to our customers.

Research and Innovation

As a technology-driven company, we continue to strengthen our research and development capabilities and regard technological innovation as a key driver of our long-term growth. By improving our research and development management and development processes, we enhance our product design capabilities and technical services to meet evolving customer needs. We also closely monitor industry technology trends and promote the continuous upgrading of our solutions through ongoing research and development investment and internal technological accumulation. In addition, we actively participate in technical forums, academic exchanges and industry seminars, strengthening collaboration with research institutions and industry partners to facilitate knowledge sharing and support technological advancement within the industry.

Supply Chain Management

We have established a lifecycle supplier management framework covering admission, performance evaluation, supervision, auditing and exit management, and are progressively integrating ESG considerations into our procurement processes. During supplier onboarding, we assess suppliers' quality assurance capability, delivery reliability, compliance performance and environmental and occupational health and safety management. During cooperation, we conduct annual audits and performance evaluations, requiring rectification where non-compliance is identified and suspending or terminating cooperation where necessary. In addition, in line with industry trends and customer expectations, we are gradually introducing practices such as green electricity use, carbon data disclosure and sustainable procurement to promote a green, transparent and sustainable supply chain.

Community Engagement

We attach importance to fulfilling our corporate social responsibilities and actively participate in community initiatives while maintaining sound operations. During the Track Record Period, we donated to charitable programs organized by the Pudong New District representative office of the Shanghai Charity Foundation to support an artificial intelligence training camp for persons with disabilities, helping to enhance their digital skills and technological application capabilities. We also established a charitable partnership with the Pudong New District Disabled Persons Party-Mass Service Center to support the continued implementation of related programs. Going forward, we will continue to support technology education and community initiatives through volunteer services and charitable cooperation, contributing to sustainable social development.

Integrity and Anti-Fraud

We regard integrity as a core component of our corporate governance and have established a comprehensive anti-fraud and anti-corruption framework. We have implemented internal policies including the Anti-Bribery, Anti-Corruption and Anti-Fraud Management System (《反賄賂反腐敗反舞弊管理制度》), the Customer-Related Process Control Procedure (《與客戶有關過程控制程序》), the Procurement Control Procedure (《採購控制程序》), the Procurement Control Procedure (Operational Management of Production Materials) (《採購控制程序(生產性產品運營)》), as well as our Code of Conduct for Employees, covering key areas such as procurement, sales, tendering and partner management. We have also established dedicated whistleblowing channels, including telephone and email, to receive reports while strictly protecting the confidentiality of whistleblowers. Any confirmed misconduct is handled under a strict "zero tolerance" policy with accountability pursued in accordance with applicable laws and regulations.

INTERNATIONAL SANCTIONS AND U.S. EXPORT CONTROL COMPLIANCE

Certain of our AI ASIC customization services involved the use of certain U.S.-origin software tools, IP, and components, and therefore required an assessment under applicable U.S. export control laws. Our international sanctions legal advisor reviewed and considered the software used in designing the chip, together with the chip's performance level, technical specifications, and all relevant IP and technical materials used in or provided for the project. After analysis, the international sanctions legal advisor concluded that these uses did not trigger any restrictions under applicable international sanctions or U.S. export control laws, including the U.S. foreign direct product rules, and that our activities do not implicate restrictions under international sanctions during the Track Record Period. In addition, certain of our suppliers may be subject to trade restrictions. For example, one of our founding partners is included on a U.S. export control list. However, our international sanction legal advisor is of the view that our procurement of founding services and materials from it does not violate the applicable U.S. export control rules as the items involved do not fall within the jurisdictional scope of these rules.

LEGAL PROCEEDINGS AND COMPLIANCE

Legal Proceedings

During the Track Record Period and up to the Latest Practicable Date, we had not been and were not a party to any material legal, arbitral, or administrative proceedings, and we were not aware of any pending or threatened legal, arbitral, or administrative proceedings against us or our Directors that could, individually or in the aggregate, have a material adverse effect on our business, financial condition, and results of operations.

Compliance

During the Track Record Period and up to the Latest Practicable Date, we had not been and were not involved in any material non-compliance incidents that have led to fines, enforcement actions, or other penalties that could, individually or in the aggregate, have a material adverse effect on our business, financial condition, and results of operations.

We are committed to fostering a culture of compliance by establishing and implementing various policies and procedures, such as comprehensive risk management procedures, to ensure that our operations consistently meet regulatory and compliance requirements.

Social Insurance and Housing Provident Fund Contributions

During the Track Record Period, with the consent of certain employees, we have made social insurance based on the agreed amounts with such employees, rather than in strict accordance with PRC laws and regulations, primarily due to varying individual preferences regarding participation levels in social benefit programs. We have not fully settled the shortfall in contributions as of the Latest Practicable Date. In 2023, 2024, and 2025, the amount of shortfall in respect of social insurance contributions was RMB5.9 million, RMB11.5 million, and RMB13.4 million, respectively.

During the Track Record Period, we also engaged third-party human resources providers to make social insurance and housing fund contributions for certain of employees, because these employees preferred to participate in local social insurance and housing fund schemes in their place of residency, which differed from the cities where their employee contracts were executed. During the Track Record Period, the contributions made by third-party human resources service provider was RMB4.3 million, RMB6.9 million, and RMB7.8 million, in 2023, 2024, and 2025, respectively. Pursuant to PRC laws and regulations, the contributions to social insurance and housing provident funds made through third-party accounts may not be viewed as fully compliant. If these third-party arrangements are challenged by the competent PRC authorities, or if the contributions are not made in full or in a timely manner, we may be required to make supplemental contributions, pay late fees or penalties, and could be subject to labor disputes.

Pursuant to PRC laws and regulations, if there is a failure to pay the full amount of social insurance as required, the social insurance premium collection department may require payment of the outstanding amount within a prescribed period, and it may charge a late fee of 0.05% per day of the delayed payment amount. If such payment is not made within the stipulated period, the competent authority may further impose a fine of one to three times of the overdue amount.

As advised by our PRC Legal Advisor, the risk of us being subject to any material administrative penalties for failing to make full social insurance contributions is remote, in the absence of material changes to current policies, regulations, and local enforcement practices, and provided that no material employee complaints arise, based on the following grounds:

(i) we have obtained certificates issued by the competent authorities for labor and social insurance and housing provident funds stating that, during the Track Record Period, we were not subject to any administrative penalties for violating laws and regulations related to labor and social insurance or housing provident funds;

(ii) the competent authorities indicated in the interview that, in regulatory practice with the absence of employee complaints or reports, they generally do not proactively conduct comprehensive investigations, impose penalties, or require back payments of historical social insurance contributions, and any complaints or reports are generally handled on a case-by-case basis;

(iii) according to the Notice of the General Office of the State Administration of Taxation on the Prudent and Orderly Implementation of Social Insurance Premium Collection and Administration (Tax General Office [2018] No. 142) (國家稅務總局辦公廳關於穩妥有序做好社會保險費徵管有關工作的通知(稅總辦發[2018]142號) which was promulgated on October 10, 2018, the tax bureaus of all provinces must prudently handle historical arrears issues, adhering to the principle of clarifying and properly taking over historical arrears accounts, without proactively organizing or carrying out arrears collection work. In addition, the tax bureaus must standardize law enforcement inspections, and must not proactively organize or carry out arrears investigations for prior years;

(iv) as of the Latest Practicable Date, we have not received any material employee complaints or regulatory notices regarding social insurance and housing provident fund contributions, nor have we been involved in material disputes or subject to administrative penalties in relation thereto during the Track Record Period; and

(v) if we receive employee complaints or regulatory orders to make such payments, we will promptly settle the outstanding shortfall in social insurance.

Based on the above, our Directors are of the view that the issues relating to the contributions of social insurance and housing provident funds would not have a material adverse effect on our business, financial condition, and results of operations.

See "Risk Factors — Risks Relating to Doing Business in Jurisdictions Where We Operate — Failure to comply with the social insurance and housing provident fund regulations in China may subject us to fines and other legal or administrative penalties."

To ensure full compliance with all statutory requirements relating to social insurance and housing provident funds, we have proactively initiated rectification measures. Our subsidiaries in Shanghai, Nanjing, and Wuxi have achieved full compliance since January 2026, and our subsidiary in Chengdu has achieved full compliance since March 2026. Furthermore, we have formulated a comprehensive rectification plan, pursuant to which we will make full and direct social insurance and housing provident funds contributions for all employees starting from April 2026.

In addition, we have implemented the following internal control measures to ensure compliance with policy and regulation requirements:

- our human resources department will regularly review and update our payroll and employee records to ensure that all contributions are calculated and made in compliance with the latest PRC laws and regulations;
- our human resources department will closely monitor the latest regulations and policies regarding social insurance and housing provident funds to prevent further non-compliance; and
- we will strengthen compliance training for our employees and management team on PRC laws and regulations in this regard.

INTERNAL CONTROL AND RISK MANAGEMENT

We are exposed to various risks during our operations. We have put in place a set of internal control and risk management policies and procedures to address potential operational, financial, legal, and market risks identified in relation to our operations. We also periodically review these procedures to ensure their effectiveness. Our policies and procedures relate to managing our research and development management, sales operations, procurement execution, financial reporting, information disclosure management, and general controls over information technology.

We have designated responsible personnel in our Company to monitor the ongoing compliance by our Company with PRC laws and regulations that govern our business operations and oversee the implementation of necessary measures. In addition, we plan to provide our Directors, senior management, and relevant employees with continued training programs and updates regarding PRC laws and regulations as appropriate with a view to proactively identify any concern and issue relating to any potential non-compliance.

We have adopted internal rules and policies governing various aspects of our business operations and management, including information systems, physical assets, procurement, sales and marketing, financial reporting, and human resources. For example, we have designed and implemented a series of internal control policies and procedures relating to our information management system, such as the establishment of a dedicated team responsible for cybersecurity and data protection, the formulation of data protection policies and measures, and the provision of training to employees involved in data control and management. In addition, we have established internal control policies covering various aspects of human resource management, such as recruiting, training, work ethics, and legal compliance. Furthermore, we have adopted a set of policies and procedures in connection with our financial reporting management, such as financial and accounting policies, budget management procedures, and financial statement preparation procedures.

During the Track Record Period, our Directors did not identify any material internal control weakness or failure. We have also engaged an independent internal control consultant to evaluate our internal control system in connection with the [**REDACTED**]. The internal control consultant has conducted review procedures on our internal control system in certain aspects, including company-level and process-level internal controls relating to financial reporting. Our internal control consultant did not identify any material internal control weakness or failure in our internal control system.

LICENSES, APPROVALS, AND PERMITS

During the Track Record Period and up to the Latest Practicable Date, we have obtained all licenses, permits, and approvals necessary for our business operations in all material respects from government authorities in China, and these licenses, permits, and approvals remained in full effect.

The following table sets forth a list of our material licenses, permits, and approvals.

License/Permit/Approval	Holder	Granting Authority	Grant Date	Expiry Date
Business License	Our Company	Beijing Economic-Technological Development Area Market Supervision and Administration Bureau (北京經濟技術開發區市場監督管理局)	February 1, 2021	—

AWARDS AND RECOGNITIONS

We have established strong brand and reputation with our technological capabilities and trustworthy services.

The following table sets forth certain significant awards and recognition that we have received.

Awarding Year	Award/Recognition	Issuing Organization
2025	2025 China Top 10 Innovative Enterprise in AI Chip (2025中國AI芯片創新十強企業)	World Integrated Circuit Association (WICA)
2025	National Standard GB/T 46280.1-2025 (Specification for chiplet interconnection interface — Part 1: General principles) (芯粒互聯接口規範第1部分：總則)	State Administration for Market Regulation (國家市場監督管理總局) and Standardization Administration of China (國家標準化管理委員會)
2025	National Standard GB/T 46280.2-2025 (Specification for chiplet interconnection interface — Part 2: Protocol layer technical requirements) (芯粒互聯接口規範第2部分：協議層技術要求)	State Administration for Market Regulation (國家市場監督管理總局) and Standardization Administration of China (國家標準化管理委員會)
2025	National Standard GB/T 46280.3-2025 (Specification for chiplet interconnection interface — Part 3: Data link layer technical requirements) (芯粒互聯接口規範第3部分：資料連結層技術要求)	State Administration for Market Regulation (國家市場監督管理總局) and Standardization Administration of China (國家標準化管理委員會)
2025	National Standard GB/T 46280.4-2025 (Specification for chiplet interconnection interface — Part 4: Physical layer technical requirements based on 2D package) (芯粒互聯接口規範第4部分：基於2D封裝的實體層技術要求)	State Administration for Market Regulation (國家市場監督管理總局) and Standardization Administration of China (國家標準化管理委員會)
2025	National Standard GB/T 46280.5-2025 (Specification for chiplet interconnection interface — Part 5: Physical layer technical requirements based on 2.5D package) (芯粒互聯接口規範第5部分：基於2.5D封裝的實體層技術要求)	State Administration for Market Regulation (國家市場監督管理總局) and Standardization Administration of China (國家標準化管理委員會)
2025	2025 China Top 20 AI Infrastructure Service Providers in Commercial Implementation (2025中國AI基礎設施服務商商業落地Top20)	EqualOcean Intelligence (億歐智庫)
2025	National Specialized and Sophisticated "Little Giant" Enterprise (國家專精特新「小巨人」企業)	Ministry of Industry and Information Technology of the People's Republic of China (中華人民共和國工業和信息化部)
2025	National High-tech Enterprise (國家高新技術企業)	Jiangsu Provincial Department of Science and Technology (江蘇省科學技術廳), Jiangsu Provincial Department of Finance (江蘇省財政廳), and Jiangsu Provincial Taxation Bureau, State Administration of Taxation (國家稅務總局江蘇省稅務局)

Awarding Year	Award/Recognition	Issuing Organization
2025	2025 China Top 20 AI Semiconductor Industry Innovation Service Provider (2025中國AI半導體產業創新服務商TOP20)	Organizing Committee of World Innovators Meet 2025, EqualOcean (億歐創新者年會2025主委會)
2025	2024 VENTURE50 New Seed List (2024VENTURE50新芽榜)	PEdaily.cn (投資界) under Zero2IPO Holdings Inc. (清科控股有限公司)
2024	2024 China Top 100 Influential Semiconductor Enterprise (2024中國半導體企業影響力百強)	World Integrated Circuit Association (WICA)
2024	2024 China Semiconductor Rising Star Enterprises Top 20 List (2024中國半導體新銳企業Top20榜單)	Organizing Committee of World Innovators Meet 2025 (創新者年會2025主委會)
2023	Jiangsu Provincial "Entrepreneurship & Innovation" Talent (江蘇省「雙創人才」)	Organization Department of the Jiangsu Provincial Committee of the CPC (江蘇省組織部) and Industry and Information Technology Department of Jiangsu (江蘇省工信廳)