*The information and statistics set out in this section and other sections of this document were extracted from different official government publications, available sources from public market research and other sources from independent suppliers, and from the independent industry report prepared by CIC. We engaged CIC to prepare an independent industry report in connection with the* **[REDACTED]** *(the "**CIC Report**"). The information from official government sources has not been independently verified by us, the Joint Sponsors,* **[REDACTED]**, *any of their respective directors, supervisors, and advisors, or any other persons or parties involved in the* **[REDACTED]**, *and no representation is given as to its accuracy. Accordingly, the information from official government sources contained herein may not be accurate.*

## I. OVERVIEW OF THE GLOBAL IC INDUSTRY

Integrated circuits (ICs) are miniaturized electronic circuits fabricated on wafers using semiconductor manufacturing processes. ICs nowadays are widely used in data centers, consumer electronics, automobile, communications, industrial and other sectors. The market size of the global IC industry reached USD677.9 billion in 2025, and is expected to increase to USD1,370.5 billion in 2030, at a CAGR of 15.1%.

### IC industry value chain

The IC industry's upstream suppliers primarily serve the midstream IC design segment by providing silicon design services, semiconductor IP, Electronic Design Automation (EDA) tools, manufacturing, and packaging and testing services, altogether translating IC specifications into physical layouts, fabricated wafers, and packaged semiconductor chips. IC design largely determines the product function, performance, manufacturing cost and other attributes of the end chip, and the design segment represents a significant source of value creation within the IC industry. The downstream includes system vendors in computer systems, communications, consumer electronics, automotives, and other sectors.

### The rise of the "design-lite" model

Since the 1960s, the global IC industry has undergone the shift through three business models. **The IDM model** used to be dominant, with companies controlling the full value chain across design, manufacturing, and packaging. With the rise of personal computing and the escalating cost of advanced fabrication, this model became increasingly unsustainable. Wafer foundries such as TSMC created **the fabless model**, where chip companies may focus on IC design while outsourcing manufacturing and packaging to partners. It reduced the capital expenditures (Capex) of chip companies and improved responsiveness to faster product cycles.

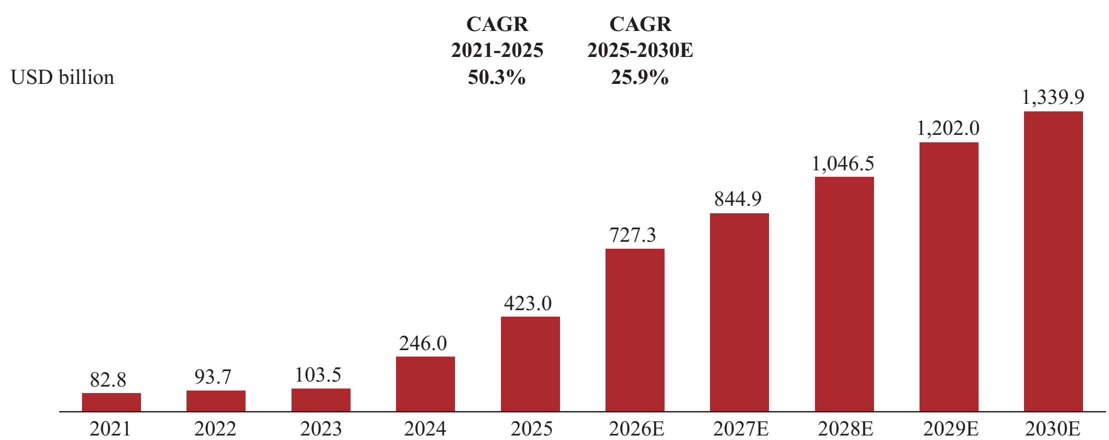
The most recent shift commenced in the 2000s and continues today, driven by the smartphone and mobile Internet revolution, and subsequent waves of smart devices. Escalating design complexity and constantly evolving architecture have increased development risk and resource requirements. Third-party design service providers, such as custom silicon service and IP providers, led the wave of **"design-lite,"** where fabless companies may further concentrate on chip definition and system architecture while outsourcing software, front-end and back-end implementation and production management to these service providers. This approach reduces operating expenses (Opex) for fabless companies whose R&D expenses could amount to 25%-30% of their revenues, improves design efficiency, and shortens time-to-market.

## II. OVERVIEW OF CUSTOM SILICON SOLUTIONS

### Rapid acceleration of global investment in AI computing

Artificial Intelligence has evolved into a structural, multi-decade global shift. Since the 2022 inflection point marked by the launch of ChatGPT, the rapid adoption of Large Language Models (LLMs) has catalyzed a fundamental transformation in computing demand. Such demand requires significant AI infrastructure support. The AI capital expenditure, led by global technology leaders such as Amazon, Google, Microsoft and Meta, nearly doubled each year from 2023 to 2025, reaching USD423.0 billion in 2025, and is expected to increase to over USD1.3 trillion by 2030.

**Global AI Capex, 2021-2030E**




### The Strategic Pivot: ASICs as the Efficiency Frontier

Unlike traditional workloads, AI computation is dominated by highly structured tensor and matrix operations. Furthermore, AI performance is increasingly constrained by data movement rather than raw compute, requiring customized memory hierarchies, high-bandwidth interconnects, and tightly integrated accelerators to optimize system efficiency. In this context, architectural specialization, in contrast to generality, plays a critical role in improving efficiency. As noted by David Patterson and John Hennessy — global pioneers in computing architecture and Turing Award winners — domain-specific architectures (DSAs) can achieve substantially higher performance and energy efficiency than general-purpose processors.

As a result, global and Chinese system vendors across the industry are pivoting to proprietary, AI-specific custom silicon, or "AI ASICs." By utilizing DSAs, ASICs optimize the total cost of ownership (TCO), delivering superior performance-per-watt and deterministic latency compared to general-purpose processors.

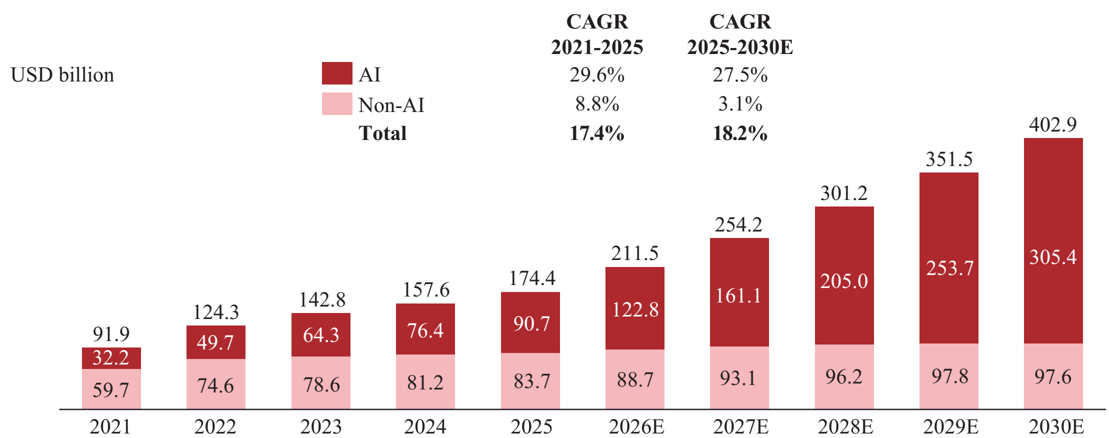
The adoption of ASICs is becoming increasingly widespread, with examples including Google's TPU, Amazon's Trainium, and Groq's LPU (which has been integrated into NVIDIA's LPX systems), among others. It is expected that approximately 40% of AI server chip shipments will be contributed by AI ASICs by 2026.

On top of that, AI ASIC deployment will expand rapidly from cloud infrastructure to edge environments. The next wave of scaling and commercialization will center on fine-tuning of vertical large models and edge inference that is tailored to domain-specific applications, such as healthcare, finance, and education. Consistent with this shift, intelligent computing chips for edge inference and fine-tuning are expected to surpass those for cloud training by 2028.

This transition spans a number of large-sized or fast-growing end-markets, such as automotive, smartphones, AI PCs and tablets, AI glasses, AI toys, and robotics, among others. For example, the global shipment of AI glasses is expected to exceed 15 million in 2026 with a year-on-year increase of more than 70%, while AI toys equipped with offline AI models are expected to begin mass-production globally from 2027 with a shipment of over 5 million in the same year. These diverse edge scenarios impose distinct semiconductor requirements, including stringent power efficiency and thermal management for battery-powered devices, ultra-low latency for real-time responsiveness, and compact form factors accommodating limited physical space. AI ASICs are well positioned to meet these requirements efficiently.

According to CIC, the global ASIC market size reached USD174.4 billion in 2025, and is expected to increase to USD402.9 billion in 2030. Therein, the AI ASIC market is growing at a significantly faster pace than the overall market.

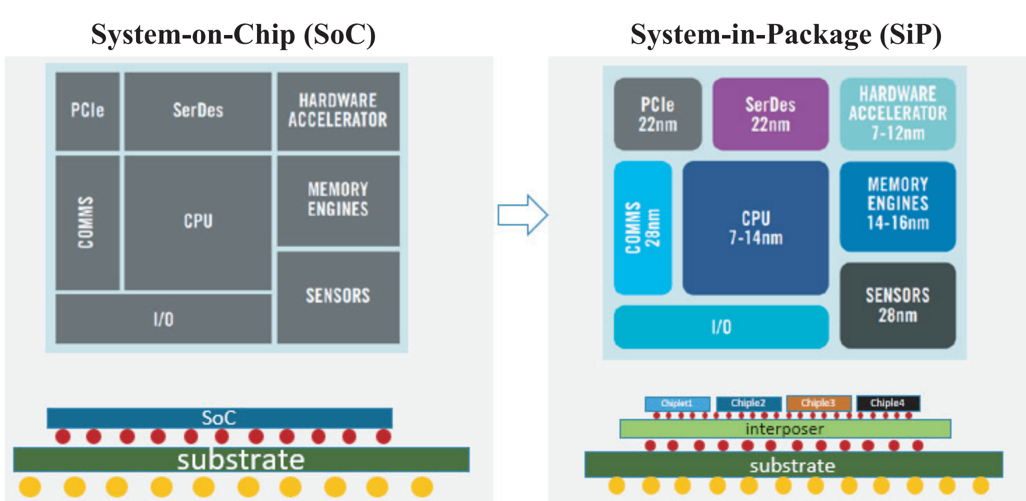
**Global ASIC market size, in terms of revenue, 2021-2030E**




*Source: WSTS, Omdia, CIC*

**Custom silicon solution providers are essential enablers of ASICs**

System-in-Package (SiP) technology has evolved from a packaging convenience into a strategic architectural pivot, essential for the next generation of high-performance computing and edge AI. Unlike monolithic System-on-Chip (SoC) designs that require every component to share a single, expensive process node, SiP enables heterogeneous integration. This modularity optimizes performance-per-watt by utilizing advanced 2.5D and 3D interconnects to minimize parasitic capacitance, effectively lowering the energy required for data movement. Furthermore, by utilizing a chiplet framework of pre-validated functional blocks, SiP drastically accelerates time-to-market, bypassing the multi-year design and verification cycles of massive single-die systems. As monolithic scaling hits the "reticle limit" and faces soaring yield-related costs, SiP provides the economic and physical path forward for "More than Moore's scaling."



While enabling higher computational density, SiP also introduces significant technical challenges for IC design companies, including increased design complexity, more demanding thermal and signal integrity requirements, and higher tape-out risk, all under shorter development timelines. In the meantime, the industry is undergoing a strategic convergence where chip companies integrate software and systems while system vendors develop proprietary ASICs to achieve vertical optimization and cost efficiency. This shift significantly accelerates the development of custom silicon solution providers, who serve as the essential bridge for system vendors to navigate the complexities of design, manufacturing and high-performance packaging. They provide chip development support from specification to mass production, including IP integration, front-end and back-end implementation, and turnkey coordination of wafer fabrication and packaging. In light of the design-lite trend, they allow customers to optimize operating expenses, focus on developing their core technical advantages, and shorten time-to-market in order to improve competitiveness.

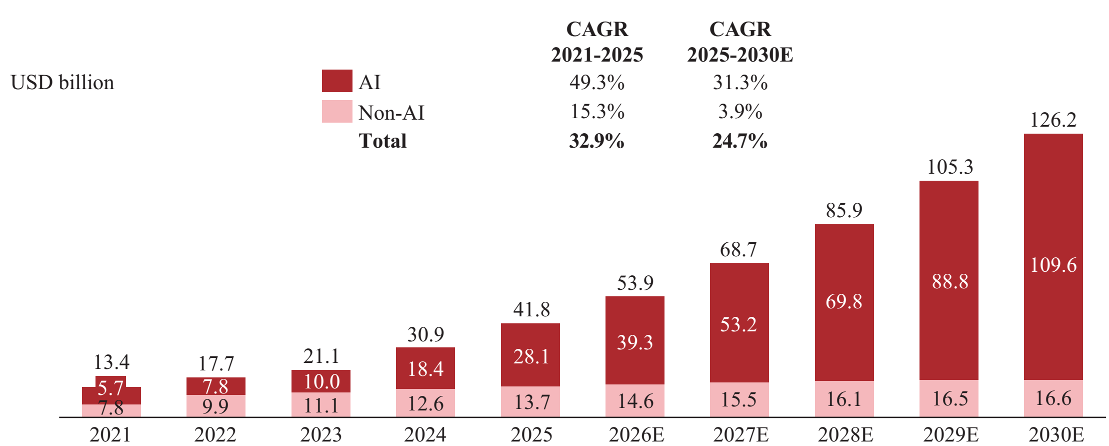
**Proven success and massive opportunities for custom silicon solution providers**

The success of this model is demonstrated globally by leading U.S. players such as Broadcom and Marvell, who derived a significant proportion of revenue growth in recent years from providing custom silicon solutions for tech giants that are developing proprietary AI ASICs, such as Google, Microsoft, Meta, Amazon, and OpenAI, among others.

Leading Chinese cloud service providers (CSPs), such as Alibaba, Baidu, Tencent and ByteDance, are also significantly increasing their investments in AI related capital expenditure, especially AI compute with their proprietary AI ASICs. This shift is expected to create a massive strategic opportunity for leading custom silicon solution providers in China.

According to CIC, the global custom silicon solution market size reached USD41.8 billion in 2025, and is expected to increase to USD126.2 billion in 2030. Therein, AI ASIC solution market size reached USD28.1 billion in 2025, and is expected to increase to USD109.6 billion in 2030, at a significantly faster growth rate compared to the overall market.

**Global custom silicon solution market size, in terms of revenue, 2021-2030E**




*Source: WSTS, Omdia, CIC*

Growth drivers of custom silicon solutions include: (i) escalating full-chip integration complexity, as modern SiPs and SoCs integrate heterogeneous compute engines, advanced memory subsystems, and high-speed interfaces, significantly increasing cross-domain coordination requirements, while many system vendors lack the in-house capability to manage end-to-end; (ii) hardware-level competitive differentiation, as system vendors tightly co-optimize chip architecture with proprietary software stacks, algorithms, and system designs to achieve superior performance and efficiency, which is not replicable with standardized processors; and (iii) value-chain control, as system vendors seek to reduce reliance on merchant silicon beyond purely performance considerations by securing access to manufacturing resources, ensuring yield and reliability, and coordinating procurement and logistics operations to enable stable delivery.

## III. OVERVIEW OF SEMICONDUCTOR IP SERVICES

### Overview of semiconductor IP

Semiconductor IP is a foundational pillar of modern IC development. It refers to pre-designed, reusable functional blocks that implement specific processing, interface, or system capabilities inside a chip. These IP blocks are integrated into SiPs and SoCs as building components rather than being re-designed from scratch, enabling faster development, lower risk, and proven functionality.

Modern chips incorporate a large number of specialized IP blocks, each responsible for distinct system functions and is indispensable to the overall chip performance. Digital IP and analog / mixed-signal and RF IP constitutes two primary semiconductor IP categories. The former implements logic-based processing and control functions that process, manage, and route digital data within an IC. The latter enables signal conversion, power management, and high-speed communication between chip components and external systems. In modern heterogeneous architectures, system performance depends not only on compute engines but also on the efficiency of data communication across the system.

### Value proposition of semiconductor IP services

Historically, leading chip companies developed most foundational IP internally, similar to how early IDMs built proprietary EDA tools before the rise of third-party vendors. However, maintaining comprehensive in-house IP capabilities across all functional domains has become increasingly impractical.

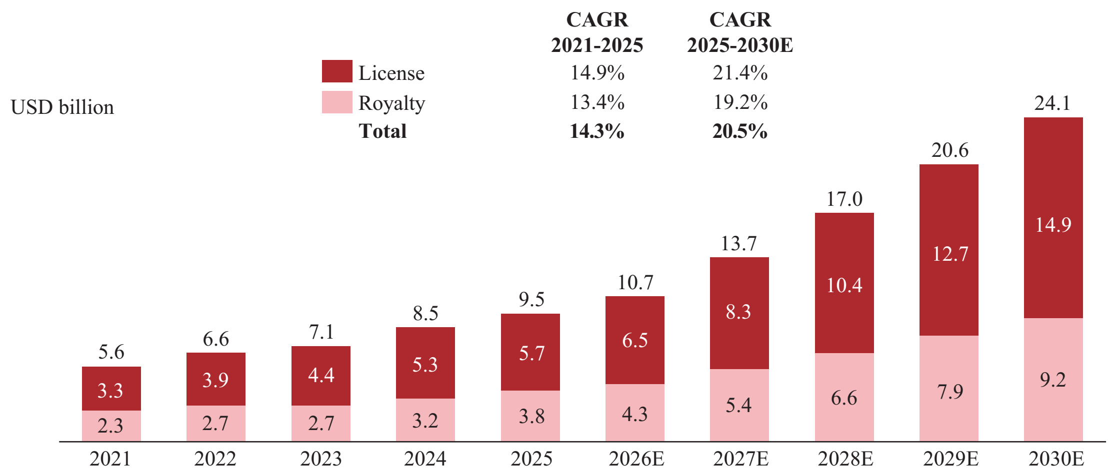
Semiconductor IP providers emerged to address this challenge by offering reusable, silicon-proven IP blocks that can be integrated directly into new designs. By licensing in these foundational but resource-intensive components, IC design companies can reduce development cost and risk while allowing internal teams to focus on system architecture, software integration, and product differentiation.

As the IC industry shifts toward the design-lite model and product cycles continue to shorten, this approach has become increasingly central to modern chip development. Reusable IP enables designers to avoid rebuilding core functions from scratch, improving development efficiency while maintaining performance and reliability.

### Market size

According to CIC, the global semiconductor IP service market size reached USD9.5 billion in 2025, and is expected to increase to USD24.1 billion in 2030, at a CAGR of 20.5%. It consists of two revenue models, namely, license and royalty. License revenue represents upfront payments for IP access typically associated with new businesses, and reflects ongoing innovation and technological advancement. Royalty revenue represents recurring payments tied to chip production volumes, providing stable income from established, silicon-proven IP that has achieved market adoption.

**Global semiconductor IP service market size, in terms of revenue, 2021-2030E**




*Source: IPnest, CIC*

Growth drivers of semiconductor IP services include: (i) expanding global IC design activity across diverse applications, which increases demand for verified interface, memory, security, and compute IP blocks; (ii) escalating verification and tape-out risks at advanced process nodes, where silicon-proven IP reduces costly design iterations and improves first-pass success rates; (iii) compressed product cycles that favor modular reuse of pre-validated IP over in-house development to accelerate time-to-market; and (iv) AI proliferation driving demand for specialized functional blocks such as NPUs, high-bandwidth memory controllers, and advanced interconnect fabrics.

## IV. COMPETITIVE LANDSCAPE

### Custom silicon solutions

Custom silicon solution providers primarily comprise two types: full-stack providers and back-end focused providers. Full-stack providers command the complete design flow from front-end architecture to back-end implementation, ensuring seamless optimization across all stages, whereas back-end focused providers are typically confined to specific foundry processes and mainly focus on back-end physical implementation tasks without architectural influence. In 2025, over 80% of the combined revenue of the world's top ten custom silicon solution providers was generated by full-stack providers.

VeriSilicon was the world's fourth largest full-stack custom silicon solution provider in terms of revenue in 2025, and the largest Chinese mainland player therein. It is also the only top five player with a highly synergistic semiconductor IP service business.

Besides, it is a pureplay provider who is solely focused on custom silicon solutions, compared to certain peers who provide merchant silicon products as their primary business. Pureplay providers remain strictly service-oriented, avoiding potential conflicts of interest with customers. This positioning, combined with a foundry-neutral approach, enhances trust, operational flexibility, and supply chain resilience.

**Ranking of full-stack custom silicon solution providers, in terms of revenue, 2025**

| Rank | Company | Global custom silicon solution revenue, USD billion, 2025 | Market share, 2025 | Pureplay provider |
|---|---|---|---|---|
| 1 | Company A | 12.80 | 30.6% | No |
| 2 | Company B | 1.23 | 3.0% | Yes |
| 3 | Company C | 1.20 | 2.9% | No |
| **4** | **VeriSilicon** | **0.33** | **0.8%** | **Yes** |
| 5 | Company D | 0.22 | 0.5% | No |

*Source: Annual reports, expert interviews, CIC*

*Notes:*

1. Company A was founded in 1961 and is based in the US. It provides semiconductor and infrastructure software solutions for data centers and networking, and is listed on Nasdaq.

2. Company B was founded in 2015 and is based in Japan. It provides custom silicon solutions, and is listed on the Tokyo Stock Exchange.

3. Company C was founded in 1995 and is based in the US. It is a fabless semiconductor company providing data infrastructure semiconductor solutions, and is listed on Nasdaq.

4. Company D was founded in 1997 and is based in Taiwan. It is a fabless semiconductor company providing system-on-chip solutions, and is listed on the Taiwan Stock Exchange.

## Semiconductor IP services

The semiconductor IP landscape can be broadly categorized into three types of players: (i) EDA vendors that offer foundational physical and interface IP as an extension of their EDA ecosystems; (ii) IP providers whose core revenues are anchored in digital IP, and in particular, processor IP, which is also often referred to as Star IP; and (iii) specialized IP providers focused on non-digital IP, such as memory and connectivity.

Digital IP occupies a central position in system architecture and compute value creation. As the AI-driven shift toward heterogeneous computing accelerates, increasingly complex IC designs demand integrated, multi-domain digital IP portfolios. An extremely limited number of providers possess the capability to deliver across multiple mainstream digital IP domains at scale.

While VeriSilicon differentiates itself with a comprehensive IP portfolio by holding the largest number of IP categories across both digital and analog / mixed-signal and RF IP, its primary revenues are anchored in digital IP. Within this type of players, VeriSilicon was the world's second largest semiconductor IP provider in terms of total IP revenue in 2025.

Besides, VeriSilicon was the world's eighth largest semiconductor IP provider in terms of total IP revenue in 2025, and the largest Chinese mainland player therein. It was also the world's sixth largest semiconductor IP provider in terms of IP license revenue in 2025. IP license revenue reflects not only the new businesses but also ongoing innovation and technological advancement.

**Ranking of semiconductor IP providers primarily focused on digital IP, in terms of total IP revenue, 2025**

| Rank | Company | Global IP revenue, USD billion, 2025 | Market share, 2025 |
|---|---|---|---|
| 1 | Company E | 4.25 | 44.8% |
| **2** | **VeriSilicon** | **0.11** | **1.2%** |
| 2 | Company F | 0.11 | 1.2% |
| 4 | Company G | 0.09 | 0.9% |

**Ranking of semiconductor IP providers, in terms of total IP revenue, 2025**

| Rank | Company | Global IP revenue, USD billion, 2025 | Market share, 2025 | Type/IP focus |
|---|---|---|---|---|
| 1 | Company E | 4.25 | 44.8% | Dominant provider of CPU architecture within digital IP |
| 2 | Company H | 1.75 | 18.5% | EDA vendor, deeply integrating physical and interface IP with foundry processes |
| 3 | Company I | 0.74 | 7.8% | EDA vendor, deeply integrating physical and interface IP with foundry processes |
| 4 | Company J | 0.28 | 2.9% | Specialized interface IP provider, focusing on high-speed memory and connectivity |
| 5 | Company K | 0.16 | 1.7% | Specialized memory IP provider, focusing on embedded memory |
| 6 | Company L (Acquired) | 0.15 | 1.6% | Specialized interface IP provider, focusing on high-speed connectivity |
| 7 | Company M | 0.12 | 1.3% | Specialized memory IP provider, focusing on embedded memory and reliability solutions |
| **8** | **VeriSilicon** | **0.11** | **1.2%** | **Comprehensive IP provider, offering a spectrum of digital IP alongside a variety of analog / mixed-signal and RF IP** |
| 8 | Company F | 0.11 | 1.2% | Domain-specific digital IP provider, specialized in DSP |
| 10 | Company G | 0.09 | 0.9% | Domain-specific digital IP provider, specialized in GPU |

**Ranking of semiconductor IP providers, in terms of IP license revenue, 2025**

| Rank | Company | Global IP license revenue, USD billion, 2025 | Market share, 2025 |
|---|---|---|---|
| 1 | Company E | 1.70 | 30.0% |
| 2 | Company H | 1.59 | 28.1% |
| 3 | Company I | 0.49 | 8.6% |
| 4 | Company J | 0.28 | 4.9% |
| 5 | Company L (Acquired) | 0.15 | 2.7% |
| **6** | **VeriSilicon** | **0.09** | **1.7%** |
| 7 | Company G | 0.06 | 1.1% |
| 7 | Company N | 0.06 | 1.1% |
| 7 | Company F | 0.06 | 1.1% |
| 10 | Company M | 0.04 | 0.7% |

*Source: Annual reports, expert interview, CIC*

*Notes:*

1. Company E was founded in 1990 and is based in the UK. It is listed on Nasdaq.
2. Company F was founded in 2002 and is based in the US. It is listed on Nasdaq.
3. Company G was founded in 1985 and is based in the UK. It is a private company.
4. Company H was founded in 1986 and is based in the US. It is listed on Nasdaq.
5. Company I was founded in 1988 and is based in the US. It is listed on Nasdaq.
6. Company J was founded in 1990 and is based in the US. It is listed on Nasdaq.
7. Company K was founded in 1995 and is based in the US. It is listed on Nasdaq.
8. Company L was founded in 2017 and is based in the UK. It was acquired by a leading SoC company during 2025.
9. Company M was founded in 2000 and is based in Taiwan. It is listed on the Taiwan Stock Exchange.
10. Company N was founded in 2003 and is based in the US. It is listed on Nasdaq.

## Competitive barriers

***Extensive silicon design platform and IP reserves.*** Broad coverage of reusable IP portfolios and proven design platforms enable scalability across different applications. This asset base shortens development cycles and strengthens competitive positioning.

***Market-proven IP portfolio.*** High-quality semiconductor IP is not developed in isolation. It is accumulated and refined through repeated silicon implementations across multiple chips, process nodes, and application scenarios. Over time, IP blocks are strengthened through silicon validation, software adaptation, system integration experience, and long-term deployment across diverse customer products. IP that has been widely implemented and market-proven is significantly more reliable than newly developed in-house alternatives.

***Technical depth and talent resources.*** Advanced chip and IP development requires multidisciplinary expertise across digital, analog, verification, and system integration. Building and sustaining such engineering depth, including hardware-software co-design capabilities that deliver superior efficiency and integration outcomes, forms a long-term barrier.

***Collaboration with industry-leading customers.*** Custom silicon solutions and IP development capabilities are refined through repeated engagements and high-volume silicon deployment. Accumulated implementation experience creates reliability advantages that are difficult for new entrants to match.

***Ecosystem partnerships.*** Established relationships with foundries and other supply chain partners enable predictable tape-out schedules and manufacturing quality. This coordination capability is critical for complex ASIC execution.

***Synergy between custom silicon solutions and IP services.*** Combining custom silicon solutions with proprietary IP creates reinforcing advantages. Design engagements refine and expand IP portfolio, while proprietary IP enhances design capabilities, strengthening long-term competitiveness.

## SOURCE OF INFORMATION

CIC was commissioned to conduct research, provide an analysis of, and to produce a report on the global IC market, and other related economic data, at a fee of RMB500,000. CIC undertook both primary and secondary research using a variety of resources. Primary research involved interviewing key industry experts and leading industry participants. Secondary research involved analyzing data from various publicly available data sources.

The market projections in the commissioned report are based on the following key assumptions: (i) the overall global social, economic, and political environment is expected to maintain a stable trend during the forecast period; (ii) certain key industry drivers are likely to continue to drive market growth during the forecast period; and (iii) there is no extreme force majeure or unforeseen industry regulations in which the market may be affected either dramatically or fundamentally during the forecast period. Our Directors confirm that, after making reasonable enquiries, there is no material adverse change in the market information since the date of the CIC Report which may qualify, contradict or have an impact on the information in this section.