OVERVIEW

Who We Are

We are a leading public company that provides custom silicon solutions, leveraging our comprehensive and proprietary portfolio of semiconductor IPs. Founded in 2001 and headquartered in Shanghai, we operate on a unique "Silicon Platform as a Service" ("**SiPaaS**") business model, offering custom silicon solution and semiconductor IP licensing services. We are well-positioned as a critical ecosystem player at the intersection of semiconductor IP, design service, and industry collaboration, enabling customers across the globe to innovate efficiently in the AI era.

According to CIC, we are a top-tier proprietary IP player, holding the largest number of IP categories across both digital IPs and analog & mixed-signal and radio frequency ("**RF**") IPs as of December 31, 2025 and are the second-largest semiconductor IP provider globally that primarily focused on digital IP in terms of IP revenue in 2025. We are also the largest IP provider in Chinese mainland and the eighth-largest globally in terms of IP revenue in 2025, and the sixth-largest global IP provider in terms of IP licensing revenue in 2025.

We are also a pioneering custom silicon solution provider, with a proven track record in delivering complex system-on-chip ("**SoC**") and system-in-package ("**SiP**") as well as low-energy and cost effective silicon design solutions. We are the world's fourth-largest full-stack custom silicon solution provider in terms of revenue in 2025, and the largest player in Chinese mainland, according to CIC. As of December 31, 2025, we have successfully executed numerous projects across a broad spectrum of process nodes, including the 4nm FinFET and 22nm FD-SOI process nodes, which illustrates the breadth and depth of our IP and design capabilities.

Our Business Model

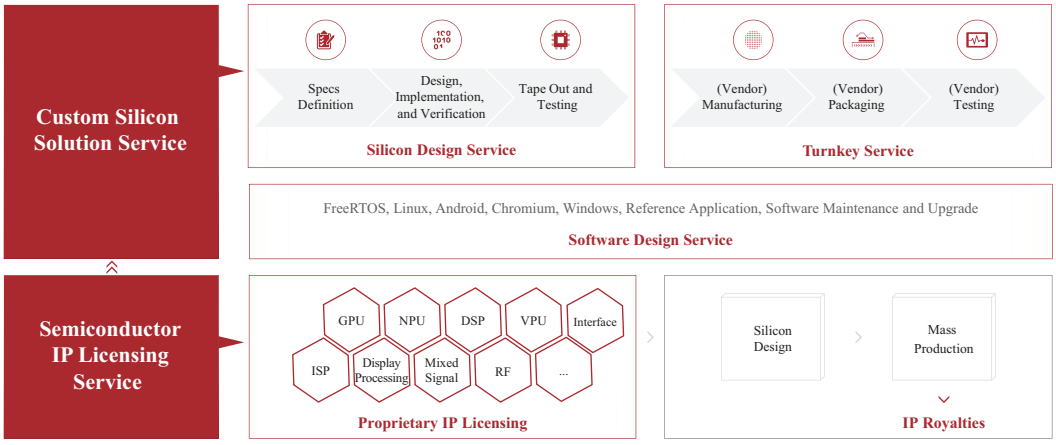
Our business model reflects the ongoing paradigm shift in the traditional semiconductor value chain. As a foundational enabler, our SiPaaS model spearheads the industry-wide shift towards "design-lite." By deeply integrating an extensive portfolio of proprietary semiconductor IPs with comprehensive custom silicon capabilities, our customers can offload their complex IC design execution and mass production processes to us. This significantly empowers both chip companies (including fabless companies and integrated device manufacturers ("**IDMs**")) and system vendors (Internet companies, cloud service providers ("**CSPs**"), automotive companies and original equipment manufacturers ("**OEMs**")), enabling them to focus on product definition and core architecture innovation while substantially lowering their operational expenditures. This model also helps insulate us from the inherent cyclicality experienced by traditional chip product companies.

SiPaaS — Silicon Platform as a Service

Our core business model is Silicon Platform as a Service (SiPaaS). Characterized by its platform-based, comprehensive, and one-stop service nature (from specification to mass production), SiPaaS provides us with a high competitive barrier.

Unlike the models of traditional fabless companies, the SiPaaS model is anchored by our extensive proprietary portfolio of semiconductor IPs, including processor IPs and analog & mixed-signal IPs (including RF IPs and interface IPs). By performing system-level optimization on these IPs, we have created a flexible and reusable design platforms. This not only significantly reduces customers' design time, costs, and risks, but also enables us to provide a complete service ranging from chip definition, front-end and back-end design, and software design, to mass production management and delivery.

In addition, unlike chip companies, our SiPaaS model does not involve manufacturing or selling proprietary branded chips. We focus on providing custom silicon solution service and semiconductor IP licensing service based on our deep technological expertise.



Our revenue is derived from two highly synergistic businesses:

Custom Silicon Solution Service

Our custom silicon solution service consists of the following two components:

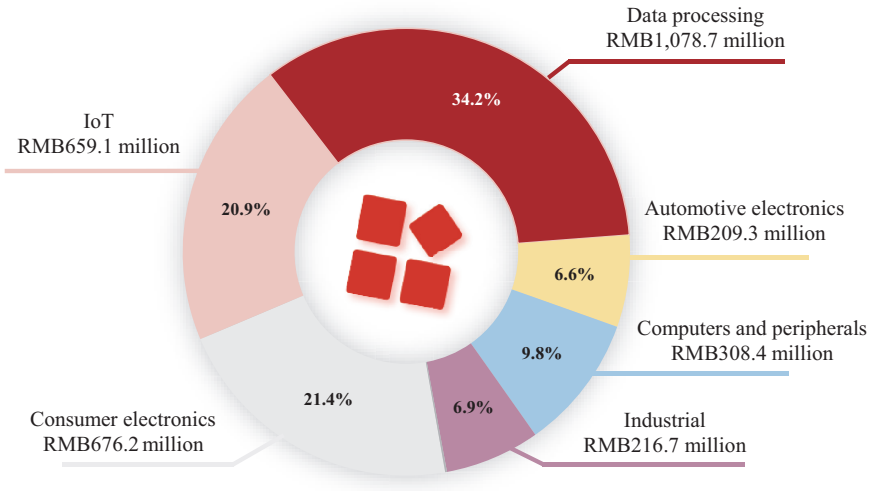
- **design service:** We provide silicon design service from specification definition to tape-out, generating non-recurring engineering (NRE) revenue. This service includes architecture definition, software design, IP selection and integration, RTL design, verification, physical implementation, and prototyping. Our platform-based model enables us to leverage our design expertise and scale that across a diverse client base, significantly enhancing design efficiency;
- **turnkey service:** We manage the entire production process from wafer fabrication to packaging, testing, and logistics, generating scalable mass-production revenue based on shipment volume. Our turnkey service is also scalable, allowing us to manage the significant growth in mass production volumes with a logistic operation team with relatively fixed size. This enables our profitability to scale across the business as our customers'production volumes increase.

Semiconductor IP Licensing Service

Our semiconductor IP licensing service is divided into two phases:

- **IP licensing:** We grant customers the right to use our IPs in their chip designs and collect licensing revenue. The substantial costs required to create our IP portfolio are incurred upfront and recognized as research and development expenses. Once validated, these IPs can be licensed repeatedly with minimum incremental costs. In alignment with increasing market demand, we anticipate our high-margin IP licensing revenue will improve our financial performance;
- **IP royalties:** We collect IP royalties based on the volume of chips shipped that integrate our IPs, forming a scalable revenue stream that grows alongside our customers' success; and as more designs incorporating our IP enter mass production, these royalties will increasingly contribute to our profitability.

Our revenue is diversified both by end-market application and by customer type. We offer our services across a wide range of applications, including data processing, consumer electronics, IoT, computers and peripherals, industrial, and automotive electronics. Our customer base includes chip companies (fabless companies and IDMs) and system vendors (Internet companies, CSPs, automotive companies and other OEMs).



Note: breakdown of revenue in 2025 by end application

From SiPaaS to AiPaaS (AI Platform as a Service)

Our business model, SiPaaS, is inherently flexible and not bound by any specific application domain. As AI becomes pervasive, this model naturally extends into AI-specific platforms — what we refer to as our AI Platform as a Service ("**AiPaaS**"), with SiPaaS remaining the core of our platform.

As shift to the AI era accelerates, we provide customers with:

- **a rich AI processor IP portfolio:** This portfolio is centered around a scalable neural network processor technology architected to deliver highly efficient computing across a full spectrum of AI workloads. Its capabilities include optimization not only for generative AI applications like large language models ("**LLMs**") and AIGC, but also for established convolution-based models and the complex mixed workloads found in real-world applications. This foundation enables a series of deeply integrated AI-enabled IPs, such as AI-ISP, AI-Display and AI-DSP. We have also launched an innovative GPGPU architecture focused on energy efficient compute and have licensed it to multiple players across the ecosystem.

Our services in this area are based on:

- **deeply integrated software and hardware co-design, as well as chip and packaging co-design capabilities:** Our hardware and software co-design approach enables the parallel development of chips and software stacks, accelerating design cycles. We also conduct silicon and packaging co-design to ensure optimal performance and reduce late-stage modifications. Our proprietary, innovative on-chip hardware acceleration service significantly optimizes the performance, power, and area characteristics of custom silicon across diverse and complex AI workloads. Concurrently, we apply our Chiplet and next-generation packaging engineering capabilities to address the increasingly complex requirements of heterogeneous computing, which is becoming more important in the AI era.
- **complete AI ASIC custom services:** Encompassing all stages from chip specification definition, front-end and back-end design, to mass production management and delivery, we provide a highly reliable complete process that shortens customers' R&D cycles.

Leveraging these core capabilities, we have established our custom silicon solutions that span:

- **cloud computing platforms:** engineered for power efficient, data-intensive processing in data centers and servers.

- **edge AI computing platforms:** delivering "always-on," ultra-low energy, ultralight spatial computing devices such as smartwatches and AI/AR glasses, AI toys, AI rings as well as high-efficiency edge computing devices such as AI PCs, AI smartphones, intelligent vehicles, and robotics.

AI ASIC presents a historic opportunity

The launch of ChatGPT in 2022 catalyzed a new era of computing demand, requiring massive AI infrastructure centered on high-performance chips. To achieve superior energy efficiency and lower latency than general-purpose processors, system vendors worldwide are increasingly pivoting to proprietary, AI-specific custom silicon solutions, or "AI ASICs."

We have successfully established ourselves as a trusted partner for leading CSPs globally, while simultaneously positioning for the emerging edge AI market, including the existing market for AI smartphones, AI PCs and AI Pads, as well as emerging markets for AI/AR glasses, AI toys, AI rings, and intelligent vehicles, among others. Our AI-related IP portfolio has scored substantial design wins, and our financial performance reflects this strategic positioning.

Cloud AI ASIC

Unlike traditional workloads, AI computation is dominated by highly structured tensor and matrix operations. Furthermore, AI performance is increasingly constrained by data movement rather than raw compute, requiring customized memory hierarchies, high-bandwidth interconnects, and tightly integrated accelerators to optimize system efficiency. As a result, CSPs are increasingly adopting heterogeneous computing architectures to manage the AI workload. This transition has catalyzed the development of proprietary AI ASICs, which offer a more cost-effective and energy-efficient alternative to general-purpose processors. CSPs are pivoting toward custom silicon optimized for specific workloads — such as training, inference, and video transcoding — to maximize performance-per-watt and achieve sustainable infrastructure expenditure. As we are targeting premium revenue streams, our shift toward direct engagement with CSPs, Internet companies and system vendors secures higher-value projects.

To address the substantial, heterogeneous workloads of modern data centers, we have established a highly competitive technology portfolio in high-performance and power-efficient GPU and GPGPU. Leveraging our proprietary unified computing architecture, we seamlessly integrate Graphics Units, Parallel Processing Units (Shaders), and AI acceleration Cores alongside a unified memory system. This architecture empowers CSPs to flexibly and efficiently deploy various tasks from complex graphics rendering to dense generative AI calculations.

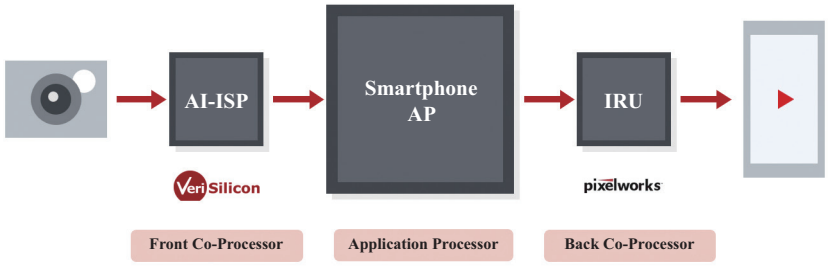
As a result, we are seeing significant revenue and robust new bookings growth, with year-over-year growth of 35.9% and 103.4% in 2025, respectively. Specifically, orders from the data processing end market accounted for over 50.0% of our new bookings in 2025 and nearly 60% of our backlog as of December 31, 2025, and both achievements were primarily driven by the strong demand for cloud-based AI ASICs and IPs. As of the Latest Practicable Date, we have provided custom silicon solution service and semiconductor IP licensing service to seven of the global top ten CSPs in 2025, according to CIC.

Edge AI ASIC

Beyond cloud infrastructure, we are well positioned to capture the significant edge AI opportunity across multiple application domains, supported by tangible market progress and our proven technical prowess.

AI smartphones: Smartphone is the largest segment in the existing edge AI market, and we have deployed a series of key solutions for its AI-driven upgrade, according to CIC. For example, our technology collaboration and integration with Pixelworks Semiconductor provides smartphones with a full-path visual enhancement solution. Our AI-ISP achieves

front-end image processing optimization, significantly enhancing the clarity, dynamic range, and environmental adaptability of images and videos. Meanwhile, Pixelworks Semiconductor's independent Image Rendering Unit ("**IRU**") specializes in back-end rendering to boost visual effects and deliver smart, smooth, and natural high-frame-rate motion graphics. This collaborative front-and-back-end architecture effectively breaks through the power consumption and thermal dissipation bottlenecks that mobile devices face in gaming and high-performance computing scenarios, offering users a markedly upgraded visual experience.



Note: illustration of synergies between AI-ISP and IRU in smartphone application

In parallel, we provide up to 40 TOPS of dedicated AI computing power per smartphone chip, and our NPU IP and AI-ISP have both achieved mass-production deployment in flagship models of leading global smartphone brands.

AI glasses: AI glasses is an emerging market where we see a significant increase in chip designs and development, according to CIC. As early as five years ago, we commenced the design of a customized, dedicated AR glasses chip for a leading global Internet company, which significantly reduced system power consumption compared to industry peers, according to CIC. By implementing precise control over independent power domains and a multi-level standby wake-up system, the chip we designed achieved optimized power efficiency and thermal management. Building upon this commercially proven technological foundation and our proprietary, optimized, low-power Nano IP portfolio, we are dedicated to providing advanced hardware solutions for the next-generation AI glasses.

AI toys: AI toys represent a high-potential market within the edge AI sector, according to CIC. We have developed two innovative on-device AI solutions tailored for children's toys based on Google's open-source Gemma3-270M lightweight language model: a visual-language model for image-based cognitive learning (for example, recognizing animals and everyday objects) and a story generation model that creates dynamic narratives. Optimized for our edge AI platforms, these models deliver real-time interaction with latency under 100 milliseconds — even in outdoor, offline environments. We finetuned the original (Gemma3-270M) model and added extra parameters in pursing for higher-quality responses and accuracy. With the total solution size under 500 million parameters, all data processing happens locally on the toy, ensuring privacy and security. Designed for children aged from three to five years old, our solutions turn playtime into an immersive, educational experience.

Intelligent vehicles: Intelligent vehicles represents the largest portion in the edge AI market in terms of output value, according to CIC. We are well positioned to capitalize on the localization trend in autonomous-driving and smart-cockpit architectures. Our competitive advantage rests on a dual-layered foundation: not only is our entire silicon-design flow ISO 26262 certified, but we also have a comprehensive portfolio of automotive-grade, functional-safety (FuSa) certified IPs, encompassing ISP, NPU, Display Processing, and Interface IP. With over a decade of experience in the automotive and market, we continue to expand in cutting-edge MCUs, smart cockpits, and Chiplet-based heterogeneous integration, aiming to provide global automotive customers with a solution spanning from IP licensing to full-chip customization.

These core autonomous driving technologies can also be leveraged into the high-growth robotics market, further illustrating the scalability of our expertise in custom silicon solutions and IP portfolio. Our ability to create functional-safety, high-performance computing platforms positions us to be a key enabler for this next wave of embodied intelligence.

Global Strategy and Ecosystem

We have established a global R&D and sales network, operating nine R&D centers (located in Shanghai, Chengdu, Beijing, Nanjing, Haikou, and Guangzhou, China; Silicon Valley and Dallas in the United States; and Ho Chi Minh City, Vietnam) and 11 sales and customer support offices worldwide as of December 31, 2025. This strategic footprint enables us to attract top talent, enhance R&D efficiency, and deliver high-quality, localized services to our customers.

Note: illustration of our global footprint

Our revenue structure also reflects our global presence: our overseas revenue accounted for 22.8% of total revenue in 2023, 36.5% in 2024, and 32.6% in 2025. We also maintain long-term collaboration with leading international customers, including Samsung, Google, Amazon, Microsoft, Baidu, Tencent, and Alibaba. Our strategic collaboration with Google is a milestone in our edge AI strategy. Based on the Open Se Cura open-source project, we jointly developed the ultra-low-energy Coral NPU IP tailored for edge LLMs. By combining Google's open-source technology with our enterprise-grade IP and custom silicon solution service, the Coral NPU provides an "always-on," ultra-low-energy and ultra-lightweight computing foundation for AI glasses, wearable devices and AI toys and similar applications. In parallel, we have established deep, long-term collaborative, relationships with leading global foundries and OSAT partners, including foundries such as TSMC, Samsung, SMIC and GlobalFoundries; and OSAT partners such as ASE Technology, Amkor Technology, JCET, and TFME.

We have strengthened our technology portfolio through strategic cross-border acquisitions, such as the DSP division from LSI Logic (2006, forming the foundation of our DSP IP) and Vivante Corporation (2016, adding market-leading high-performance and power-efficient GPU IP to our IP portfolio). We are committed to international standards and open collaboration. We actively participate in and co-build global and domestic industry organizations, including the China RISC-V Industry Consortium (CRVIC), Shanghai Open Processor Industry Innovation Center (SOPIC), RISC-V International, OpenHW Group, Chips Alliance, and the UCIe Alliance.

Financial Performance

Benefiting from our unique business model, we achieved strong financial performance during the Track Record Period. Our revenue amounted to RMB2.3 billion, RMB2.3 billion and RMB3.1 billion in 2023, 2024, and 2025, respectively, with 2025 reflecting a significant year-over-year growth of 35.9%. In second half of 2025, our revenue amounted to RMB2.2

billion, representing an increase of 56.8% compared to the second half of 2024 and 124.3% compared to the first half of 2025.

Our new bookings in the second, third, and fourth quarters of 2025 reached RMB1.2 billion, RMB1.6 billion, and RMB2.7 billion, respectively, breaking our historical record for single-quarter new bookings three times. Notably, our new bookings in the fourth quarter of 2025 grew by 70.2% compared to those in the third quarter. In 2025, the total value of new bookings was RMB6.0 billion, a year-over-year increase of 103.4%. Among these new bookings, AI computing-related orders accounted for over 73%, and data-processing end market orders accounted for over 50%, primarily driven by cloud-based AI ASICs and IPs.

As of December 31, 2025, our backlog reached RMB5.1 billion, representing a substantial increase of 54.5% from RMB3.3 billion as of September 30, 2025, and up 111.0% from RMB2.4 billion as of December 31, 2024. This metric has remained at a comparatively high level for nine consecutive quarters. Among our backlog as of December 31, 2025, turnkey service exceeded RMB3.0 billion. Based on the contractual terms of the orders comprising our backlog, we expect over 80% of our backlog as of December 31, 2025 to be converted to revenue within one year, and nearly 60% of the backlog as of December 31, 2025 is from the data processing end market, primarily driven by cloud-based AI ASICs and IPs.

The IC design industry is characterized by long investment cycles and heavy R&D expenditure, according to CIC. We consistently maintain high R&D investments to build a high competitive barrier ensuring our leading chip design and technology R&D capabilities in the semiconductor IP and custom silicon fields. The net losses recorded during the Track Record Period were the result of deliberate, strategic investments in R&D, where we strategically emphasized campus recruitment to maintain and expand our R&D talent pool and avoided layoffs to preserve our competitive edge during semiconductor downturn from 2022 to 2023, as we anticipated that the emergence of Generative AI would unlock massive potential for custom integrated circuits. In 2023, 2024, and 2025, our R&D expenses accounted for 40.7%, 53.8%, and 41.7% of our revenue, respectively. These foundational investments were essential to strengthen our comprehensive semiconductor IP portfolio and establish from specification to production custom silicon capabilities, creating high barriers to entry and positioning us for long-term growth in the AI era. As our robust orders translate into execution, our previously invested R&D expenditures are progressively deployed into customer projects; and generating output, driving a reasonable downward trend in our R&D expense ratio. From 2024 to 2025, our R&D expenses as a percentage of revenue decreased by 12.1%, demonstrating the continuous optimization of our operational efficiency and the emergence of economies of scale.

OUR COMPETITIVE STRENGTHS

A unique SiPaaS business model amplifying synergies and delivers structural advantages

The rapid adoption of AI across cloud and edge accelerates the industry's shift toward "design-lite" operating models, increasing the strategic importance of semiconductor IP and design services. According to CIC, we are a leading public company that provides custom silicon solutions, leveraging our comprehensive, proprietary portfolio of semiconductor IPs, making our integrated business model a core competitive strength.

Our custom silicon solution and IP licensing services are highly synergistic, creating a virtuous cycle. For customers, using our proprietary IPs in custom silicon projects provides significant cost and design efficiencies. At the same time, our profound understanding of these proprietary IPs empowers us to deliver highly optimized custom silicon solutions. This real-world execution, in turn, yields direct market insights to continuously refine our IP portfolio. Among our custom silicon solution service customers, approximately 50% also utilized our own proprietary IP in their projects, demonstrating the strong synergy in which our custom silicon solution service drives adoption of our IP portfolio.

Our business model amplifies these synergies through inherent structural advantages:

Reusability and scalability: Our verified IPs can be licensed repeatedly with minimal incremental cost, while our IP royalties revenues scale up as our customers' chips move into mass production. Our custom silicon solutions are inherently reusable — by building on our platform and tailoring the design to specific customer's needs, we can significantly improve the efficiency of chip customization, thereby enhancing operating leverage in both the design and mass production phases. Design projects that enter mass production will generate scalable revenue for us. As of December 31, 2025, we had served approximately 350 customers for our custom silicon solution service. In 2025, 114 projects had entered the mass production stage, and additional 48 projects were pending mass production.

Expansion of customers and end market applications: We offer a one-stop suite of highly flexible service options and combinations, spanning from IP licensing, chip definition, front-end and back-end design, to mass production management. Through our configurable-on-demand IPs and services, we have cultivated a broad customer base — including chip companies (fabless companies and IDMs) and system vendors (Internet companies, CSPs, automotive companies and other OEMs) — across diverse application scenarios. This diversified reach helps mitigate the adverse effects of market volatility.

Counter-cyclical resilience: The broader semiconductor industry has historically undergone cyclical fluctuations. During industry downturns, IC design companies typically adopt a prudent strategy — focusing on research and development to develop new products in anticipation of market recovery. Furthermore, as part of their cost efficiency measures, they often increase their partnerships with third party providers such as ourselves. Industry downcycles can also provide windows for strategically acquiring semiconductor IPs. Consequently, our unique SiPaaS model demonstrates robust resilience, unlocking substantial growth potential and strategic opportunities even amid broader semiconductor industry downturns.

Our advanced and comprehensive semiconductor IP portfolio

We have built the most comprehensive proprietary IP portfolio in the global semiconductor IP industry according to CIC, spanning six major families of processor IPs (GPU, NPU, VPU, DSP, ISP and Display Processing) and more than 1,700 analog & mixed-signal IPs (including RF IPs and interface IPs). According to CIC, we are a top-tier proprietary IP player, holding the largest number of IP categories across both digital and analog & mixed-signal as of December 31, 2025 and the second largest semiconductor IP provider primarily focused on digital IP in terms of IP revenue in 2025. We are the largest IP provider in Chinese mainland and the eighth largest IP provider globally in terms of IP revenue in 2025. We are also the sixth-largest IP provider globally in terms of IP licensing revenue in 2025.

As of December 31, 2025, our NPU IP has been licensed to 91 customers and integrated into over 140 AI chips, with cumulative shipments of nearly 200 million units. Our GPU IP has been deployed for over 20 years, with customer chips that incorporate our GPU IP shipping more than 2 billion units globally. Our VPU IP has been adopted by seven of the global top 20 CSPs, three of the top five Internet companies in China and five of top eight NEV manufacturers in China, according to CIC.

The following chart sets forth our core IP adoption highlights as of December 31, 2025.

Core IP Portfolio Adoption Highlights

Global track record of high-volume deployment across diverse applications

To explore escalating demands for heterogeneous computing in the AI era, we have pioneered AI-accelerated subsystems (AI-ISP, AI-Display, AI-DSP) that leverage our proprietary FLEXA synchronous interface for ultra-low-latency, DDR-less data exchange. These innovations are already in mass production — our AI-ISP powers flagship smartphones. We have also launched an innovative GPGPU architecture and have licensed it to multiple high-performance computing chip developers.

In addition to digital IPs, we also provide a broad portfolio of analog & mixed-signal IPs (including RF IPs and interface IPs), complemented by customized IP services. Our mixed-signal services span a wide range of process nodes — from mature 250nm CMOS nodes to advanced 4nm FinFET and 28/22nm FD-SOI nodes as detailed in the table below.

Foundries	Mixed-Signal IP												
	4nm	5nm	6nm	14nm	22nm	28nm	40nm	55nm	65nm	90nm	110nm	130nm	180nm	250nm
TSMC			✓			✓	✓	✓	✓	✓		✓	✓	✓
Samsung	✓	✓		✓		✓							✓	
IBM									✓					
SMIC						✓	✓	✓	✓	✓	✓	✓	✓	✓
FUJITSU								✓						
ST						✓								
GF					✓	✓	✓	✓	✓		✓	✓		
UMC						✓	✓	✓	✓				✓	
HEJIAN											✓		✓	✓
HH Grace											✓	✓	✓	✓
HLMC								✓						
CSMC												✓	✓	
Silterra											✓		✓	

Note: illustration of mixed signal IP process node

Leveraging our strategic deployment of ultra-low-energy technologies, we have developed over 60 analog & mixed-signal IPs on the 22nm FD-SOI process node to date. This portfolio encompasses foundation IPs, data converter IPs, and interface IPs. We have cumulatively licensed FD-SOI IP cores over 300 times to 45 customers as of December 31, 2025. Furthermore, we have provided custom silicon solution service for 45 FD-SOI projects to our customers, 36 of which have successfully achieved production as of December 31, 2025.

Addressing the diversified application scenarios of the IoT, we have established a comprehensive portfolio of RF IP and platform solutions on the 22nm FD-SOI process node. This portfolio supports a variety of IoT connectivity technologies, including dual-mode Bluetooth, Bluetooth Low Energy, NB-IoT, multi-channel GNSS, and 802.11ah. All of our RF IPs have been adopted in customer chips, with those incorporating our 802.11ah, 802.15.4g, and GNSS RF IPs already in mass production.

We have also established a strong presence in interface IPs. We offer a complete interface IP product portfolio, with core achievements covering 4nm UCIe PHY and controller IPs, USB PHY and controller IPs, MIPI D-PHY/C-PHY/A-PHY PHY and controller IPs, HDMI PHY and controller IPs, DP/eDP PHY IPs, as well as PCIe PHY and high-speed SerDes IPs. The majority of our interface IPs have been integrated into multiple products for customers and have achieved mass production. Additionally, our MIPI C/D-PHY TX/RX IPs have attained ISO 26262 certification and are applied in multiple ADAS chips.

Strong custom silicon capabilities from specification to mass production

We are the world's fourth-largest full-stack (from chip specification definition to mass production) custom silicon solution service provider in terms of revenue in 2025, and the largest Chinese mainland player in that segment, according to CIC. Our design capabilities span advanced 4nm FinFET and 22nm FD-SOI to traditional 250nm CMOS process nodes, covering mainstream and specialty processes at major global foundries. We adhere to a dual-engine strategy in our technology roadmap: we apply FinFET to application scenarios requiring sustained high computing performance, while precisely targeting FD-SOI at edge computing and IoT scenarios that are extremely sensitive to power consumption. We have successful tape-out experience on process nodes from 14nm to 4nm FinFET and 28nm/22nm FD-SOI.

Through our close relationships with leading global foundries and OSAT partners, we can support customers with flexible capacity access and next-generation packaging solutions. Our design approach — leveraging reusable, silicon-proven architectures — reduces development cycles and execution risk while ensuring consistent quality.

We provide a full suite of software support services (development platforms, SDKs, customized software, and maintenance) that shorten customers' R&D cycles and reduce development risk. Our hardware-software co-design approach enables parallel development of chips and software stacks, accelerating design cycles. For advanced Chiplet and 3D-IC projects, we conduct packaging co-design from the architecture stage to ensure optimal performance and reduce late-stage modifications.

Our design flow has been certified under ISO 26262 for automotive functional-safety, and we have developed functional-safety SoC platforms and high-performance automotive SoC platforms that have been validated in customer projects.

Global presence with strong and expanding industry ecosystem partners across the industry chain

We operate as a global platform that collaborates closely with ecosystem partners to empower customers' domestic, regional, and global strategies. Our worldwide customer base spans a diverse spectrum of industry players, comprising both chip companies (fabless companies and IDMs) and system vendors (Internet companies, CSPs, automotive companies and OEMs). This extensive customer base gives us insight into technology trends in AIGC, robotics, intelligent vehicles, and next-generation consumer electronics, which in turn sharpens our strategic focus and strengthens our technical and business capabilities. Furthermore, our deep and long-term collaboration with top-tier customers has also enhanced recognition of our custom silicon solution service and reinforced our reputation. Our overseas revenue accounted for 22.8%, 37.5% and 32.6% of total revenue in 2023, 2024 and 2025, respectively.

We adopt a foundry-neutral and OSAT-neutral strategy, enabling collaboration with all major global foundries and OSAT partners without being constrained by any single partner's roadmap. As of December 31, 2025, we have close relationships with eight of the top ten global foundries and nine of the top ten OSAT partners, securing stable capacity and working on a broad spectrum of packaging technologies. We also cooperate with leading IP and EDA providers to build an advanced design-delivery system.

We are deeply committed to cultivating the semiconductor industry ecosystem. By continually hosting and participating in high-profile industry forums, we empower the supply chain and drive the commercialization of technologies. As of December 31, 2025, we have hosted 15 editions of the VeriSilicon CEO Forum, issuing five major industry development predictions annually to provide strategic market guidance. We have also hosted 15 editions of the Songshan Lake China IC Innovation Forum, through which we recommended 135 domestic ICs with a historical mass-production rate of approximately 94%. Furthermore, we have organized 10 editions of the Shanghai FD-SOI Forum, fostering deep connections among key participants across the global supply chain. In emerging technology sectors, we hosted four editions of the Dishui Lake China RISC-V Industry Forum (through which we recommended over 40 domestic RISC-V chips, and among those promoted in the first three editions of the forum for which statistics are available, more than 90% have entered mass production) and actively participated in the 5th China RISC-V Industry Forum.

Continuous R&D investments driving innovation and technological advancements

Deep early-stage R&D investment forms the cornerstone of our business, and by aligning our forward-leaning R&D with long-term end-market forecasts, we have established a proven track record of delivering market-ready innovation at the optimal inflection point. Core examples include:

FD-SOI (Investments since 2015): As semiconductor processes shrank below 28nm, severe power leakage became a physical bottleneck restricting the industry. To address this challenge, FinFET and FD-SOI technologies were introduced simultaneously. FinFET uses a 3D transistor structure to control leakage, whereas FD-SOI retains the traditional 2D planar

structure but lays an ultra-thin insulating layer (buried oxide) underneath to eliminate leakage from the source. This unique 2D architecture gives FD-SOI a natural advantage in integrating RF functions, along with extremely low power consumption.

Based on our forward-looking anticipation of edge AI scenarios' application demands, we have developed over 60 analog & mixed-signal IPs at the 22nm FD-SOI process node, provided custom silicon solution service for 45 FD-SOI projects (36 of which have been mass-produced), and have completed over 300 IP licensing to 46 customers as of December 31, 2025.

RISC-V (Investments since 2018): RISC-V is an open-standard instruction set architecture. Based on open-source principles, RISC-V allows developers to modify it freely, and its most prominent feature is its modular design. This extremely high flexibility enables chip designs to achieve an optimal balance of performance, power, and cost, thereby significantly lowering the barrier to chip design and accelerating the pace of innovation across various emerging applications, from smart wearables to AI accelerators.

Leveraging our keen insight into the trend of open-standard ISAs, we entered the RISC-V field very early, empowering the entire ecosystem with our comprehensive IP portfolio and custom silicon solution service. As of December 31, 2025, our semiconductor IPs have been adopted in 14 chips by major RISC-V chip companies, and our custom silicon solution services have been utilized by 42 customers, and 25 RISC-V chip projects have successively entered mass production as of the same date.

Chiplet (Investments since 2020): As the cost of manufacturing a single large-area monolithic chip rises sharply and yields are constrained, Chiplet technology offers a breakthrough solution — disaggregating a complex system into multiple smaller functional dies, also known as Chiplets. These Chiplets can be manufactured separately using the cost-effective process nodes, and then assembled into a complete chip through advanced packaging technologies. This approach significantly improves manufacturing yields, lowers R&D costs, and accelerates time-to-market.

We were among the first Chinese mainland enterprises to join the UCIe Alliance (2022), as part of our strategy to be at the forefront of innovation that address our customers' continuously growing demands in the era of heterogeneous compute, particularly for cloud and intelligent driving applications.

Beyond these technology focus areas, we maintain long-term, intense investment in research and development, with R&D expenses representing 40.7%, 53.8% and 41.7% of our revenue in 2023, 2024 and 2025, respectively. Alongside our commitment to organic R&D innovation, we have executed multiple successful asset and technology acquisitions globally. Through exceptional cross-cultural corporate management, we have achieved a deep and seamless integration of top-tier global technical teams and our core local talents. As of December 31, 2025, we employ 1,839 R&D personnel, accounting for 89.4% of our total workforce, with 88.4% holding a master's degree or above. In Chinese mainland, 25.0% of our employees have work experiences of over a decade, and the average employee age is approximately 32, establishing a highly qualified talent structure that balances profound experience with innovative vitality. Our sustained high R&D investment and highly efficient global talent integration is a foundational structure that allows us to continuously generate a rich portfolio of globally competitive R&D achievements.

Experienced management team and sustainable talent culture

Our founder, Dr. Wayne Wei-Ming Dai, is a renowned scientist and entrepreneur. He received his Bachelor's degree in Computer Science and his Ph.D. degree in Electrical Engineering from the University of California at Berkeley, and formerly served as a tenured full professor in the department of Computer Engineering at the University of California at Santa Cruz. He received the NSF Presidential Young Investigator Award from the President of the United States in 1990. In the academic field, he was the founding Chairman of the IEEE Multi-Chip Module Conference and IEEE Symposium on IC/Package Design Integration. He was also an associate editor of *IEEE Transactions on Circuits and Systems* and an associate editor of *IEEE Transactions on VLSI Systems*, having published more than 100 papers in technical journals and conferences as of December 31, 2025. Dr. Wayne Wei-Ming Dai was the

founder, chairman of the board of directors, and Chief Executive Officer of Ultima Interconnect Technology, Inc., and later served as the Co-Chairman and Chief Technology Officer of Celestry Design Technologies, Inc., an EDA company, which was acquired by Cadence Design Systems in 2002. Currently, his roles include a member of Asia Chancellor's Council at University of California, Berkeley, and President of Berkeley Club of Shanghai.

Under Dr. Wayne Wei-Ming Dai's leadership, we have built a highly experienced core management team, with team members possessing an average of 20 to 30 years of profound industry experience across semiconductor design, process technology, EDA/IP, software systems and supply chain. Core executives have previously served at top-tier global technology enterprises and professional institutions, including Broadcom, AMD, Marvell, Cadence, LSI Logic, HP, Bell Labs, and KPMG. This collective expertise fortifies us with management characterized by global vision and top-tier execution capabilities.

We regard talent as our core asset. Our corporate culture is built around the core values of "Fair, Care, Share, Cheer," supported by systematic technical training, transparent promotion mechanisms, and a competitive compensation system. We adhere to high standards in talent selection. Substantially all of the new graduates hired by our Group in 2025 hold master's degrees from top universities, mostly Project 985 or Project 211 universities in China. In the context of the AI era, our talent assessment evaluates not only intelligence and emotional qualities but also focuses on employees' execution capability and esthetic appreciation.

Our talent team maintains a high degree of stability. According to CIC, our voluntary turnover rate in Chinese mainland was 2.8% in 2025, significantly lower than the semiconductor industry average of approximately 10.2%. Our talent strategy has garnered widespread industry recognition, earning awards such as "Employer of Excellence" in China, "Excellence in Employee Care Plan," "Best Training Practice," and "Best Employer in the Chip Industry" for five consecutive years.

OUR GROWTH STRATEGIES

From IP to AI-enabled IP

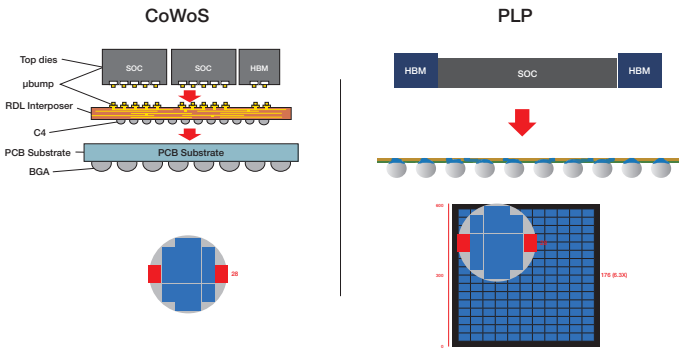
Based on our extensive proprietary semiconductor IP portfolio and R&D expertise, we are systematically upgrading semiconductor IP from traditional processing units to AI-enabled architectures. We achieve this advancement upgrading through our self-developed FLEXA synchronous interface communication technology. With this technology, we have constructed tightly coupled AI subsystems, including AI-ISP, AI-Display, and AI-DSP. These subsystems provide low-latency, high-efficiency processing pipelines, which are critical for edge AI applications. We will continue to iterate and enhance these technologies while accelerating their industrialization and commercial adoption.

From SoC to SiP

Our strategic priority is to further build our leadership in SiP and Chiplet design, leveraging our expertise across a range of next-generation packaging technologies such as Chip-on-Wafer-on-Substrate ("**CoWoS**") and panel-level packing ("**PLP**").

As the semiconductor industry undergoes a structural shift toward heterogeneous integration to meet the performance, power, and cost requirements of AI and other complex workloads, SiP, which integrates multiple Chiplets into a single package, has become a critical enabler for our customers.

To support this shift, we are building design capabilities across multiple next-generation packaging technologies. Whilst we continue to support established approaches such as CoWoS, a cornerstone of our forward-looking strategy is our pioneering investment in next-generation PLP. PLP is an emerging technology that utilizes large rectangular panels instead of round wafers, offering potential advantages in manufacturing throughput and cost, with thermal and reliability characteristics that are well-suited for demanding applications such as automotive. By strengthening our expertise in SiP and Chiplet architectures, we enable our customers to overcome the limitations of legacy monolithic SoC design, helping them achieve their specifications and accelerate time-to-market for their most advanced products.



Note: illustration of CoWos and PLP technologies

From cloud AI ASIC to edge AI ASIC

Recognizing the industry-wide shift of AI inference from centralized cloud environments to distributed edge devices — driven by imperatives for lower latency, reduced cost, and enhanced data privacy — we are aligning our capabilities to empower this transition. We intend to equip high-volume existing markets, such as AI smartphones AI PC, and AI Pads, with high-efficiency data processing and AI inference solutions. Concurrently, for emerging application areas like AI glasses, AI toys, AI rings and intelligent vehicles, we will collaborate with ecosystem partners to deliver comprehensive, optimized and low energy consumption edge-side intelligent solutions.

Deepening global ecosystem collaboration

We plan to continue to deepen our ecosystem within the global semiconductor industry by continuously expanding our partner network. On the supply chain front, we will uphold our foundry-neutral and OSAT-neutral collaboration strategies regarding foundries and OSAT partners, continuing to work closely with leading global manufacturing partners. By coordinating scaled resource pools, we are dedicated to effectively mitigating industry risks associated with capacity shortages and price fluctuations. At the same time, we will actively promote synergy between next generation packaging technologies and chip design to provide our customers with highly cost-effective and supply-secured custom silicon solution service.

Building upon a highly synergistic hardware foundation, we will further expand our strategic collaborations with global technology leaders in frontier application areas. In the rapidly evolving AI sector, we will continue to collaborate deeply with Google on "Project Open Se Cura" — an open-source framework aimed at accelerating the development of secure and efficient edge AI systems — dedicating ourselves to the development of edge-AI "Tokenization" technologies. As demonstrated by our forward-looking deployment in the AI glasses domain, we are committed to achieving hardware-software co-optimization between underlying chip architectures and small models, specifically aiming to overcome the severe power and thermal bottlenecks faced by edge computing. Furthermore, by optimizing vertical domain model solutions for specific application areas, we aim to accelerate the commercialization of advanced AI technologies across various edge scenarios.

Additionally, long-term industry ecosystem building and talent incubation are crucial for maintaining our strategic depth. We will continuously drive the robust development of international technology ecosystems such as RISC-V, FD-SOI, and UCIe, actively hosting and participating in globally influential industry exchange events, such as the RISC-V Summit China and technical seminars jointly organized with the Khronos Group. Concurrently, to continually inject fresh talent into the industry ecosystem, we will sustain initiatives like the "VeriSilicon Cup" National Embedded Software Development Competition. Through this layered progression and deep collaboration across the three dimensions of supply chain, frontier applications, and industry ecosystem, we aim to continuously consolidate our pivotal role within the global semiconductor ecosystem.

Continued investment in talent and active fulfillment of corporate social responsibility

We regard talent as our core asset and the foundation of our growth. By building a future-ready organizational structure and strengthening our employer brand, we have established a full-cycle talent management system — covering attraction, motivation, development, and retention — to foster strong connections through our corporate culture. We recruit both top scientists and outstanding graduates, deepen partnerships with leading universities, and continuously expand and upgrade our talent pool. Aligned with employee development needs, we optimize compensation and performance systems and offer competitive equity incentives to align individual growth with company success, thereby improving per capita efficiency. Our integrated training programs — both online and offline — focus on enhancing the technical and managerial capabilities of key employees and core technical staff. We are also accelerating the integration of AI tools across operations to help our people stay ahead of technological trends and drive overall efficiency. Backed by years of technical expertise, industry insight, and practical experience, we are committed to attracting and developing versatile design talent and supporting their long-term growth. In doing so, we aim to build a sustainable and resilient talent ecosystem that serves as a solid foundation for our long-term business success.

We will also continue to uphold our ESG philosophy of "Governance & Compliance, People-Centricity, Igniting Innovation, and Caring for the Planet," while comprehensively advancing our corporate social responsibility practices.

Pursuing M&A and strategic investment

Through M&A and strategic investment, we aim to acquire key IPs and technologies that are highly aligned with our strategic development directions. We also plan to leverage the Hong Kong capital market for cross-border investments and acquisitions to strengthen our technical advantages and customer coverage in overseas markets.

We will prioritize quality assets in application-specific domains that exhibit long-term growth potential and high technical barriers. Through these targeted initiatives, we intend to further expand our technology portfolio, accelerate revenue growth, and broaden our addressable markets, thereby creating long-term value for shareholders.

As of the Latest Practicable Date, we have not identified any specific targets nor entered into any definitive agreements; implementation of this strategy will be contingent upon valuation, diligence and regulatory approvals.

OUR BUSINESS

We are a leading public company that provides custom silicon solutions, leveraging our comprehensive, proprietary portfolio of semiconductor IPs. We operate under our SiPaaS model and utilize our comprehensive IP portfolio and advanced R&D capabilities to deliver custom silicon solution service and IP licensing service to a broad customer base, including chip companies (fabless companies and IDMs) and system vendors (Internet companies, CSPs, automotive companies and other OEMs). Our services are deployed across a wide range of end markets, including data processing, consumer electronics, IoT, computers and peripherals, industrial and automotive electronics. The following tables set forth our revenue by service, end-application and AI and non-AI applications.

	Year ended December 31,					
	2023		2024		2025	
	RMB	*%*	*RMB*	*%*	*RMB*	*%*
	(in thousands, except for percentages)					
Custom silicon solution service						
Design service	492,470	21.1	724,794	31.3	876,558	27.9
Turnkey service	1,071,416	46.0	856,214	37.0	1,489,681	47.3
Subtotal	**1,563,886**	**67.1**	**1,581,008**	**68.3**	**2,366,239**	**75.2**
Semiconductor IP licensing service						
IP licensing	655,375	28.1	632,859	27.3	671,253	21.3
IP royalties	109,692	4.7	103,109	4.5	110,911	3.5
Subtotal	**765,067**	**32.9**	**735,968**	**31.8**	**782,164**	**24.8**
Total	**2,328,953**	**100.0**	**2,316,976**	**100.0**	**3,148,403**	**100.0**

	Year ended December 31,					
	2023		2024		2025	
	RMB	*%*	*RMB*	*%*	*RMB*	*%*
	(in thousands, except for percentages)					
Data processing	314,718	13.5	552,201	23.8	1,078,735	34.3
Consumer electronics	513,007	22.0	484,939	20.9	676,157	21.5
IoT	961,432	41.3	642,553	27.7	659,092	20.9
Computers and peripherals	197,413	8.5	323,891	14.0	308,406	9.8
Industrial	185,718	8.0	98,254	4.2	216,705	6.9
Automotive electronics	156,665	6.7	215,138	9.3	209,308	6.6
Total	**2,328,953**	**100.0**	**2,316,976**	**100.0**	**3,148,403**	**100.0**

	Year ended December 31,					
	2023		2024		2025	
	RMB	*%*	*RMB*	*%*	*RMB*	*%*
	(in thousands, except for percentages)					
AI	1,007,075	43.2	1,295,363	55.9	2,030,989	64.5
Non-AI	1,321,878	56.8	1,021,613	44.1	1,117,414	35.5
Total	**2,328,953**	**100.0**	**2,316,976**	**100.0**	**3,148,403**	**100.0**

Custom Silicon Solution Service

We undertake all or part of the processes from chip specification definition to mass production and provide related software design service. Leveraging our semiconductor IP resources and silicon design capabilities, we help our customers reduce design risks, shorten design cycles and accelerate time-to-market. The semiconductor IPs used in our design service can also be licensed to customers on a standalone basis under our semiconductor IP licensing service.

We categorize our offerings under custom silicon solution service into (i) design service and (ii) turnkey service.

Design Service

We provide customers with services for processes from design specification definition through engineering sample production and validation, based on their requirements in terms of chip function, performance, power consumption, die size and cost. Our design service covers the full chip design flow, including:

- **design specification definition and IP selection.** Based on customers' product specification requirements, we refine and confirm chip design specifications, including IP selection, customization of certain IPs, target functional and performance indicators, and chip architecture schemes.
- **architecture design, implementation and verification.** Based on the agreed chip design specifications, we carry out architecture design and design implementation, including IP procurement and customization, logic design, design integration, functional verification, prototype validation, physical implementation, and package and test design. During the design process, we set design review milestones in accordance with the chip design specification document and the agreed review plan, and conduct regular or milestone-based reviews with customers on project progress and stage deliverables. Following review, we and the customer decide whether to proceed to the next stage. If

changes to the chip design specifications are required, we update the design specifications upon mutual agreement and adjust the design plan accordingly.

- **tape-out and engineering sample production.** After design completion and passing the internal tape-out review, the project enters the engineering sample trial production stage. We deliver design data to the selected foundries and packaging and testing service providers for wafer fabrication and engineering sample packaging and testing to complete engineering sample production.
- **sample validation and acceptance.** Following completion of engineering sample production, we work with customers' design and system teams to carry out sample testing and validation against the agreed specifications. After we and our customer have reviewed and confirmed that the samples meet the specifications, we typically complete the acceptance process and sign sample confirmation documents.
- **software design support.** In parallel with chip design, we provide software design for customers as part of the same project. Depending on the customer's specifications, this may include developing application software, software development platforms and SDKs as well as providing customized software, ongoing maintenance and upgrade services. Software projects are managed through an agreed review plan with defined design milestones. At each milestone, we review project status and interim deliverables together with the customer and agree whether to advance to the next phase. Where the customer's software requirements change, we adjust the design plan by mutual agreement and reflect those changes in the subsequent development work.

As of December 31, 2025, we had 104 design projects in execution, of which approximately 60.6% were from 28nm to 4nm process node, approximately 34.6% were from 14nm to 4nm process node, and approximately 24.0% were from 7nm to 4nm process node, reflecting our growing exposure to advanced process design projects.

Our revenue from our design service is primarily derived from providing custom silicon design service to customers, including chip specification definition, IP selection, design, implementation and verification, as well as prototype tape-out in cooperation with foundries, based on customers' requirements for performance, power consumption, size and cost.

Turnkey Service

We provide customers with services covering part or all of the processes from production planning to final delivery of wafers or chip products, by arranging outsourced wafer fabrication, packaging and testing, and providing production management services. After completion and validation of chip design and software, customers place production orders for chips based on their assessment of end-market demand; these orders typically specify, among other things, the name, specifications, quantity and unit price of the mass production chips.

In our turnkey service arrangements, we provide the following services:

- **outsourced wafer fabrication.** We place orders with qualified foundries for wafer fabrication in accordance with customers' mass production requirements, process nodes and scheduling needs, and arrange for wafers to be manufactured in line with the agreed technical specifications and quality requirements.
- **outsourced packaging and testing (OSAT).** We engage qualified packaging and testing service providers to carry out packaging and testing of wafers. We may use different packaging and testing solutions according to product needs, including to meet automotive-grade or other high-reliability requirements.
- **production management and scheduling.** We formulate production plans based on customer orders, decompose such orders into orders to various outsourced suppliers and arrange product manufacturing. We monitor production status at each stage (including progress and relevant data), regularly report production

status to customers, and, where production needs or conditions change, coordinate customers and outsourced suppliers to adjust production plans, investigate the causes of changes and help ensure stable production.

- **delivery and acceptance.** Upon completion of manufacturing and testing and confirmation that the wafers or chips meet the agreed specifications and quality requirements, we manage delivery of wafers or packaged and tested chips to customers in accordance with the agreed delivery terms, and assist customers in completing their acceptance processes where required.

We adopt a foundry-neutral and OSAT-neutral strategy, enabling collaboration with all major global foundries and OSAT partners rather than being constrained by any single partner's capacity. We have design capabilities across mainstream semiconductor processes including traditional CMOS, advanced FinFET and FD-SOI. This foundry-neutral capability enables us to help customers select optimal process and architecture solutions that balance performance, power, area and cost. Revenue from our turnkey service depends on the production scale of our customer's chips.

Selected Case Studies

Company A

Company A is one of the leading electric vehicle manufacturers in China and is at the forefront of autonomous driving and smart cockpit technologies. Since 2023, we have provided Company A with IP licensing service, including VPU IP and Dewarp IP, as well as custom silicon solution service for its autonomous driving chips. Leveraging our IP portfolio and design capabilities, Company A has developed a 5nm autonomous driving chip with high computing power. As Company A's technology roadmap in autonomous driving continues to advance, we are cooperating with it on the development of its next-generation autonomous driving chip.

Our services for Company A have been adopted in mass-produced vehicle models, providing strong computing power support and functional differentiation for the ongoing enhancement of its autonomous driving capabilities.

Company B

Company B is a provider of wireless home security systems, and its main products are intelligent security cameras for home use and video doorbells. It was acquired by a globally-renowned Internet company in 2018.

In 2017, we customized a chip on FD-SOI process node for Company B for its battery-powered home security cameras, which rely on Wi-Fi for data transmission and therefore require ultra-low-energy. As part of this project, we also designed an ultra-low-energy analog IP for Company B.

Following its acquisition in 2018 and building upon our track record of cooperation, we seamlessly extended this strategic partnership to the acquirer, empowering it with two subsequent-generation customized chips to drive the continuous evolution of its smart home camera and video doorbell products. For these new chips, we adopted more advanced low-power technologies and further upgraded the relevant IP to reduce power consumption and improve yield. In addition, our collaboration with the acquirer has expanded to software design service. Such products have achieved strong market acceptance expanding from the North America to Europe, with cumulative shipments exceeding 120 million units as of December 31,2025.

Semiconductor IP Licensing Service

Under our semiconductor IP licensing service, we license to customers:

- processor IPs, including GPU IP, NPU IP, VPU IP, DSP IP, ISP IP, Display Processing IP and AI-enabled IP.

- analog & mixed-signal IPs (including RF IPs and interface IPs), which in aggregate amount to over 1,700 IPs as of December 31, 2025.
- customized IPs, where we develop or finetune IPs to meet specific customer requirements.

Our revenue from IP licensing represents revenue generated from granting customers the right to use our self-developed semiconductor IPs, either on a stand-alone basis or as part of an IP platform. Revenue from IP royalties represents revenue generated from the use of our IPs by customers in the production and sale of their products, which is typically calculated based on units sold or a percentage of sales at an agreed-upon rate.

RESEARCH AND DEVELOPMENT

Our R&D activities are primarily driven by market trends and customer requirements, and are focused on, processor IPs, IP subsystem, analog and mixed-signal IPs, including RF IPs and interface IP, and software platforms, as well as key design methodologies. These R&D-driven capabilities allow us to apply advanced manufacturing processes and packaging that support the delivery of custom design projects under our SiPaaS business model. We rely on a combination of patents, trademarks, copyrights, know-how, confidentiality agreements and other measures to protect our intellectual property and proprietary technologies. As of December 31, 2025, our research and development efforts have produced 240 invention patents, three utility model patents, two design patents, 12 software copyrights, 151 registered trademarks, and 273 registered IC layout-design rights.

R&D Process

Custom Silicon Solution Service

Our R&D for custom silicon solution focuses on design methodologies for reusable design platforms and functional subsystems built around IP. By integrating our proprietary IP or third-party IP, we develop design platforms tailored for different application scenarios and apply these platforms in the implementation of customer projects. Each design platform typically comprises functional subsystems, associated design and verification methodologies, and implementation flows for specific process nodes. The development of these platforms generally follows a staged process, including requirements gathering, project initiation, R&D execution, project acceptance and subsequent roll-out, with the results primarily used for pre-research and continuous improvement of our design platforms.

Our software development supports the implementation of our solutions. Our software development process generally includes requirement analysis, formulation of software specifications, development planning, software architecture design, software development, code review and testing, software quality review, and software release. We have established automated testing procedures and quality control processes to support rapid and continuous software iteration and release and to ensure the delivery of software in accordance with customer requirements.

IP licensing service

Our semiconductor IP development process generally includes product market research, technical feasibility analysis, formulation of product specifications, development planning, IP architecture design, IP design implementation, IP design verification, IP performance testing and final design acceptance.

Our IP and IP Platforms

We have built a comprehensive semiconductor IP and IP platform portfolio that serves as the core technology foundation for both our custom silicon solution service and our semiconductor IP licensing service. Our portfolio covers six categories of processor IPs (GPU IP, NPU IP, VPU IP, DSP IP, ISP IP and Display Processing IP), together with more than 1,700 analog & mixed-signal IPs (including RF IPs and interface IPs). These IPs can be licensed to customers on a standalone basis or combined into subsystem- and platform-level solutions. Leveraging our SiPaaS model, we continuously upgrade and expand our IP and IP

platforms to support new AI application scenarios, advanced process technologies and Chiplet-based architectures, thereby enhancing the scalability and reusability of our technology outputs.

Graphic Processing Unit ("GPU") IP

Our GPU IP is built on more than two decades of continuous R&D, featuring a highly scalable architecture that supports efficient graphics rendering and high-performance parallel computing. The architecture covers applications ranging from ultra-low-energy wearable devices to high-performance and power-efficient GPU and GPGPU server products.

In graphics processing, the power-efficient design of architecture of our GPU IP enables complex gaming, smooth user interfaces and high-quality visual experiences across a variety of end devices. In parallel computing, our GPU architecture provides high-performance and power-efficient GPGPU capabilities to support server and data center workloads, enabling scalable computing solutions across consumer, automotive and cloud infrastructure markets.

Our GPU and GPGPU IPs have been licensed to multiple customers worldwide. They have been widely adopted in smart wearable products and hold a significant share of the global smartwatch market. In the automotive sector, our GPU IP has been integrated into tens of millions of vehicles, supporting instrument clusters, in-vehicle infotainment systems and smart cockpit platforms with the cumulative shipments of customers' chips equipped with our GPU IP exceeding two billion units, as of December 31, 2025.

Desktop

Smartphone

Automotive

PC

Data Center

Cloud Gaming

Neural Network Processing Unit ("NPU") IP

Our NPU IP is built on a hybrid architecture that combines the programmability of GPGPU with the efficiency of dedicated domain-specific accelerators. This architecture enables highly optimized neural network processing and supports a wide range of AI workloads, including computer vision, speech processing, image enhancement and large language model inference.

With performance of up to 40 TOPS, our ultra-power-efficient NPU can support complex on-device reasoning tasks, such as LLM execution, within the power constraints of edge devices. Customers' chips employing our NPU IP are already in mass production and have been deployed in smartphones of a global renowned smartphone brand as of the Latest Practicable Date.

As of December 31, 2025, our NPU IPs have been integrated into more than 140 AI chips by 91 customers, covering over ten key markets including AIoT, smartphones, intelligent driving, PCs and data centers, and customers' chips equipped with our NPU IP have been shipped nearly 200 million units worldwide.

AIoT/Smart Home

Wearables

Intelligent Driving

Smartphone

Data Center

Robotics

Video Processing Unit ("VPU") IP

With over 20 years of continuous development, our VPU IP provides advanced multi-format video encoding and decoding capabilities. It delivers high-quality, high-performance and low-power video processing to meet the stringent requirements of consumer, automotive and cloud applications.

VPU IP architecture is designed to adapt efficiently to different device constraints. In the wearable market, our VPU offers ultra-low-energy and high silicon efficiency for highly constrained devices. Leveraging our high-throughput and high-quality video processing technology, our VPU IPs are also optimized for cloud and data center infrastructure, supporting large-scale video streaming, transcoding and AI video workloads.

Our VPU IP has been widely deployed. In the automotive market, it has been adopted by 5 of the 8 emerging automotive companies to power digital cockpit, infotainment and intelligent display systems in 2025, according to CIC. In the cloud computing sector, it is used by 7 of the global top 20 cloud platform providers and 3 of the top 5 Internet companies in China in 2025, according to the same source. As of December 31, 2025, customers' chips equipped with our VPU IP have been shipped for more than 250 million units.

Surveillance/Webcam

Smart Home/Large Screen

Intelligent Driving

Data Center

PC

AI/AR Glasses

Digital Signal Processing ("DSP") IP

With over two decades of development, our DSP IP is an advanced architecture optimized for complex signal processing workloads. It delivers high data throughput and ultra-low execution latency and is specifically tailored for efficient audio, voice and communication baseband processing.

This highly configurable architecture provides deep optimization for compute-intensive workloads, including computer vision and embedded artificial intelligence, and is designed to deliver strong performance and energy efficiency across a wide range of multimedia, wireless connectivity and IoT applications.

Our latest fifth-generation DSP IP series enables flexible and scalable solutions for smart devices, automotive systems, wearables and AIoT products. The architecture is engineered to provide an optimized balance of computing capability, power efficiency and silicon area for edge devices.

Computer Vision

AIoT

Audio/Voice

Wireless & 5G

Robotics

AI/AR Glasses

Image Signal Processing ("ISP") IP

Our ISP IP is a core imaging engine designed to efficiently support multi-sensor systems and high-resolution imaging with ultra-low-energy. It is intended to enable AI vision solutions across a wide range of applications, including machine vision, intelligent vehicles, robotics, webcams, security cameras and AR/VR devices.

The ISP IP architecture integrates advanced image processing technologies, providing full support for HDR, multi-frame noise reduction, lens distortion correction and multi-sensor synchronization. For autonomous driving applications, ISP IP features an ultra-low-latency pipeline that minimizes the time from image capture to AI processing to support real-time decision-making. Our ISP IP has been certified under ISO 26262 for automotive functional-safety.

As of December 31, 2025, our ISP IP, which serves the smart home, security, automotive and embedded vision markets, had been adopted by more than 80 customers worldwide, including over 20 automotive companies.

Camera System

Automotive

Robotics

Drone

AI/AR Glasses

Doorbell

Display Processing IP

Our Display Processing IP is designed to efficiently process pixels across a wide range of display types using built-in advanced picture quality enhancement technologies. It provides a comprehensive display solution that scales from ultra-low-energy wearable displays to high-performance multi-screen systems and supports up to 8K@60fps ultra-high-definition output.

Display Processing IP integrates a broad set of display processing features, including image enhancement, super-resolution, 3D LUT color correction and support for high dynamic range standards such as HDR10, HDR10+, delivering accurate and high-contrast visual experiences. For automotive applications, our Display Processing IP has been certified under ISO 26262 for automotive functional-safety.

Our Display Processing IP has been widely deployed in mass-produced products across multiple market segments, including wearables, smartphones, tablets, smart displays and high-end consumer devices. In addition, our functional-safety-certified Display Processing IP has been deployed in mass-produced vehicles globally.

Intelligent Cockpit

Smartphone/Tablet

Smart Home

Smart Watch

AI/AR Glasses

Data Center

Image Rendering Unit ("IRU")

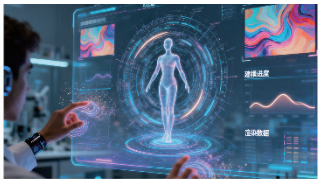
In January 2026, we completed the acquisition of a controlling interest in Pixelworks Semiconductor and added its IRU to our IP portfolio. See "History, Development and Corporate Structure — Major Acquisitions, Disposals and Mergers — Acquisition of Pixelworks Semiconductor." IRU is a proprietary visual computing technology to accelerate graphics rendering and enhance visual output quality in modern computing systems. Designed to complement traditional GPU pipelines, our IRU adopts a distributed rendering architecture comprising an image-based rendering engine for frame generation efficiency, a neural rendering engine for AI-enhanced visual details, and an enhancement engine for wide-color-gamut and HDR output.

By offloading and optimizing specific rendering tasks from the main processors, IRU technology can significantly reduce the computational burden on CPUs and GPUs. Under selected workloads, this architecture has demonstrated the capability to significantly improve system-rendering performance, enabling high-framerate and high-fidelity visual applications while maintaining device power efficiency.

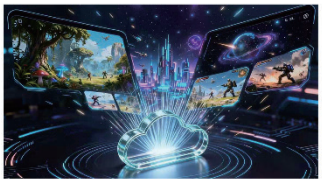
To provide comprehensive system-level solutions, we have established strategic integration between the IRU technology and our core processing engines, including our proprietary GPU, NPU, ISP and VPU IPs. This synergistic co-optimization enables customers to deploy a complete suite of AI-driven visual computing workloads across imaging, graphics and video applications with sustained performance.

Game Rendering

Video Content Creation



3D Reconstruction



Cloud Rendering Services

Robotics

Smart Display

AI-enabled IP

Our AI-enabled IP represents a cross-domain converged computing architecture optimized for edge applications. Utilizing our proprietary FLEXA synchronous interface technology, it integrates independent IP cores, such as the ISP, VPU and NPU, into tightly coupled AI subsystems.

AI-enabled IP architecture optimizes traditional in-chip data transfer by enabling direct data flow between IP cores without accessing DDR memory. This subsystem-level approach is designed to reduce memory bandwidth bottlenecks and to deliver low-latency, power-efficient processing tailored for edge AI scenarios.

Our AI-enabled IP, including the AI-ISP and AI-Display subsystem, have been deployed across various edge applications, primarily in smartphones, wearable devices and security IoT products.

AI Smartphone

Intelligent Cockpit

AI PC

Data Center

Wearables

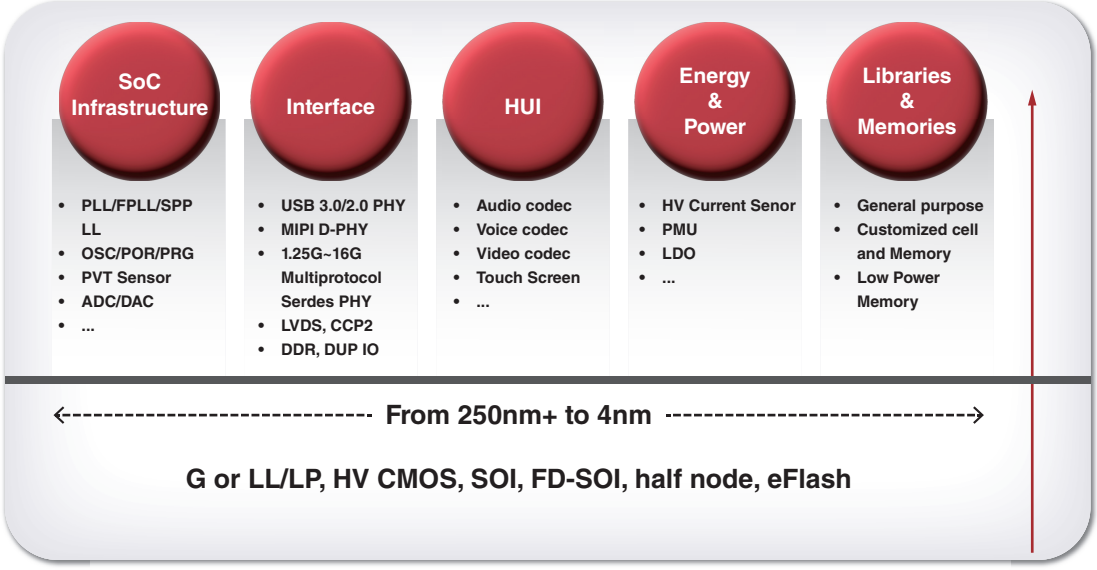
Surveillance System

As of December 31, 2025, we have developed over 1,700 mixed-signal IPs (including RF IPs, interface IPs and application-oriented analog & mix-signal IP platforms) that support a wide range of process technologies across major foundries. This extensive IP library enables our customers to streamline silicon development and accelerate product time-to-market.

Analog & mixed-signal IP

We provide a comprehensive portfolio of analog and mixed-signal IPs to support custom silicon design. This portfolio includes SoC infrastructure IP, interface IP, human-user interface IP, energy & power IP, and libraries & memories IP. These IPs can be licensed to customers on a standalone basis or integrated into subsystem and platform-level solutions.

Our silicon-proven IP portfolio is adapted to the manufacturing processes of mainstream global foundries, with coverage extending from mature process nodes down to 5nm and 4nm advanced process nodes. By supplying reliable underlying physical building blocks, these solutions are designed to help customers mitigate physical design risks when migrating to advanced nodes.

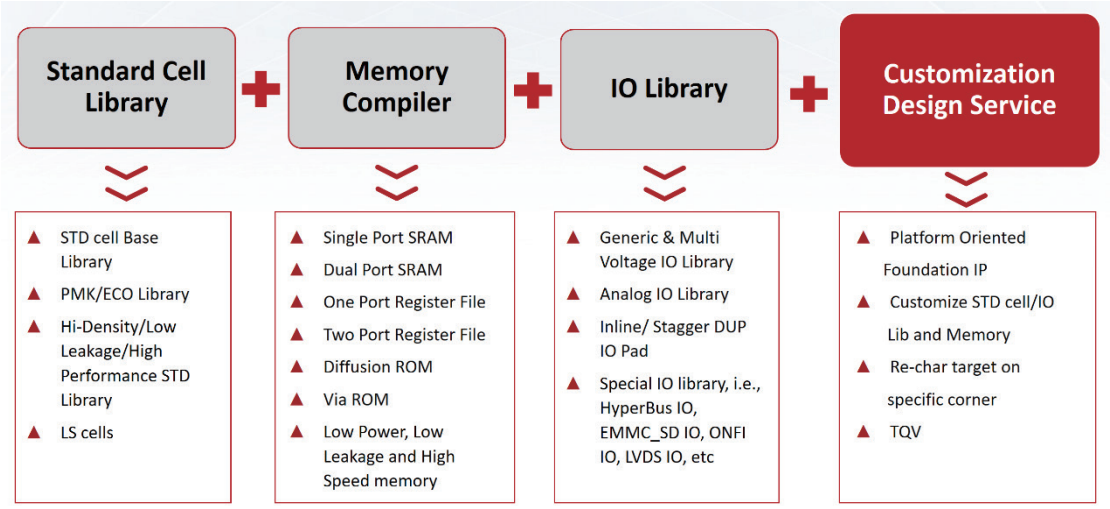


Foundation IP Platform

We design and provide a comprehensive portfolio of foundation IP, encompassing standard cell libraries, memory compilers and input/output libraries. These essential physical building blocks are designed to support a wide range of semiconductor manufacturing processes across multiple global foundries.

Our engineering capabilities include the custom re-characterization of standard cell libraries, allowing us to fine-tune physical IP to meet specific system-level requirements and to optimize for targeted processing speeds and stringent power consumption profiles in complex SoC designs.

As of December 31, 2025, the standard cells library have been deployed across a broad spectrum of process nodes. Our silicon-proven portfolio spans from 250nm mature CMOS process nodes down to advanced 5nm and 4nm FinFET process nodes from various foundries, providing a reliable physical foundation for custom silicon development.

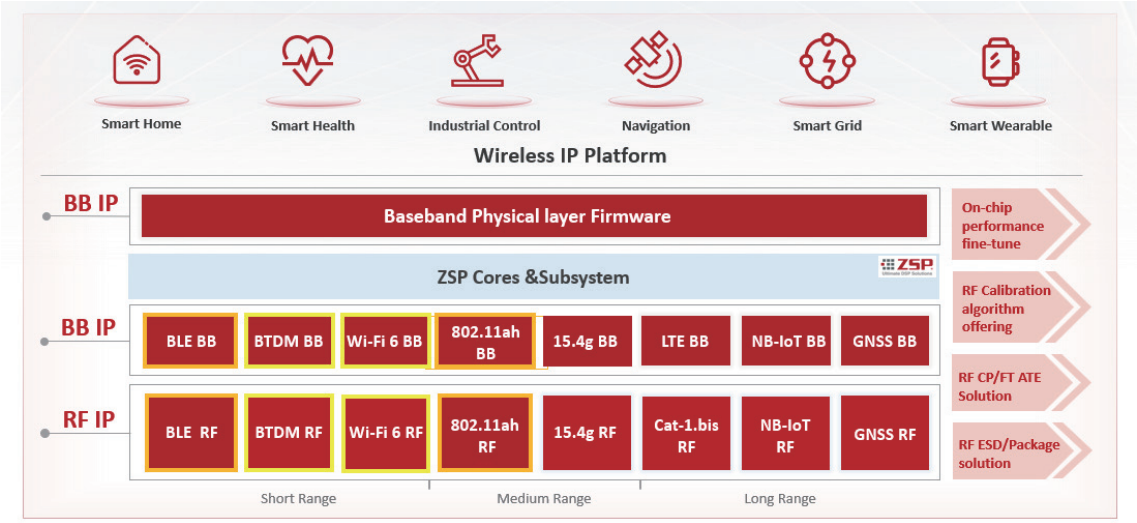


Radio Frequency ("RF") IP and Wireless Connectivity Platform

We offer full-stack wireless connectivity solutions that encompass the RF front end, baseband and software protocol stack. Developed on the 22nm FD-SOI process node, this platform provides high integration and optimized power consumption for wireless communications. Our portfolio also includes a fully developed point-to-point WiFi Aware IP, which integrates a complete RF, baseband and software stack.

This platform is compatible with mainstream wireless communication protocols, including Wi-Fi 6, BLE 5.3, NB-IoT and multi-mode satellite navigation. It incorporates on-chip performance-adaptive fine-tuning and RF calibration algorithms to help ensure reliable signal transmission. In addition, our Wi-Fi Aware IP reduces discovery and connection times and adopts a simplified software architecture to achieve power savings during standby and discovery phases.

As of December 31, 2025, this series of RF IPs has been adopted by multiple customers for mass production. In particular, our wireless solutions have been deployed in low-power consumer electronics, including smartwatches and AI/AR glasses.

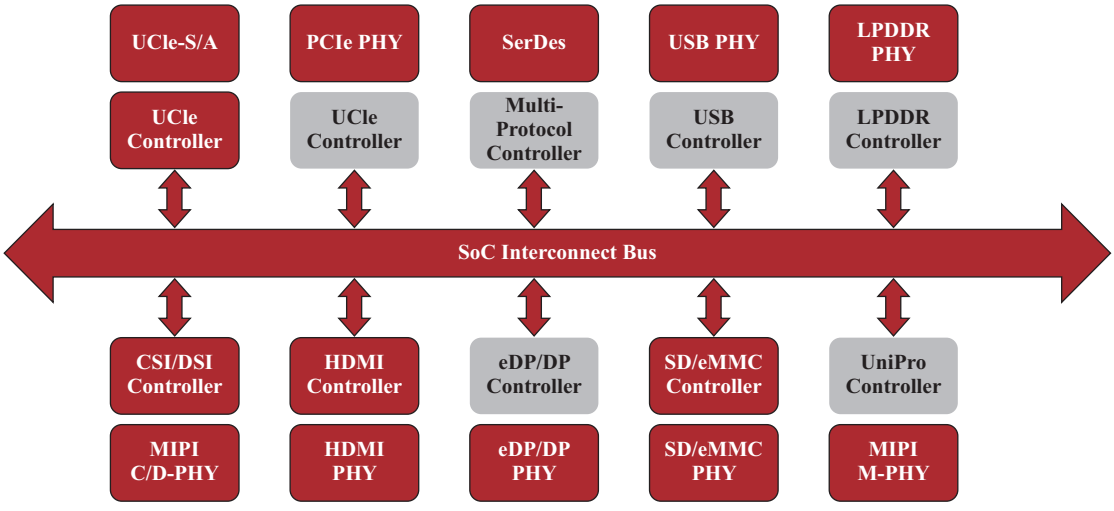


Interface IP Platform

We provide an interface IP portfolio designed for high-speed data transmission and system interconnection. This portfolio covers key industry standards, including UCIe, MIPI, USB, HDMI and PCIe, and has been ported to advanced process nodes such as 8nm and 4nm to support custom silicon development.

These interface IPs are engineered to deliver high bandwidth with low power consumption, enabling efficient data exchange both within an SoC and between external devices. This architecture is designed to meet the spatial constraints of consumer electronics as well as the reliability requirements of enterprise-level and automotive-grade applications, and serves as a critical interconnection component for heterogeneous computing and intelligent vehicle architectures.

We are currently advancing the functional-safety certification of our interface IP portfolio in a systematic manner. By leveraging an ISO 26262-certified design flow with our automotive-grade IP portfolio, we continue to deploy our interface IP solutions in the automotive electronics sector to support next-generation vehicle platforms.

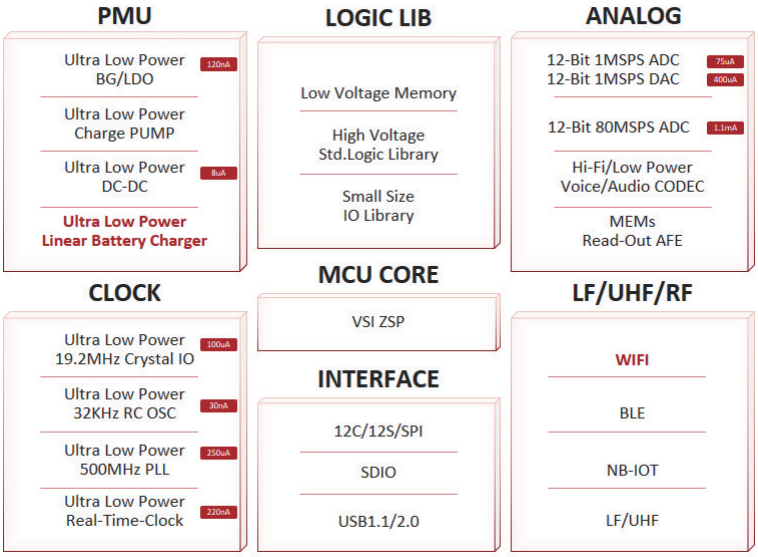


Customized Mixed-signal IP Platform

We provide analog and mixed-signal IP customization services, including high-performance analog-to-digital converters (ADC), digital-to-analog converters (DAC) and other specialized functional blocks. These services are designed to deliver tailored IP solutions that are aligned with customers' specific system architectures.

The customization process combines our analog design expertise with targeted application requirements. This enables us to address specific performance metrics and power consumption profiles that standard, general-purpose IPs may not meet, and to ensure that the IP satisfies precise operational parameters at the silicon level.

Our customization capabilities form an integral part of our SiPaaS model. By providing tailored analog and mixed-signal solutions, we enable customers to implement customized chip designs and support their specific semiconductor product development lifecycles.



High Performance SoC Platform

Our high-performance SoC platform is a system-level chip architecture developed on advanced process nodes. This platform integrates multi-core CPUs , GPUs, NPU and NoC to support high-performance computing requirements.

This architecture is designed to manage complex heterogeneous computing workloads efficiently by synchronizing different processing units to balance high-throughput computation with optimized power consumption and system scalability. The platform is structured to support the hardware requirements of high-end application processor chips.

Our high-performance SoC platform has been successfully adopted by customers' flagship tablets multimedia devices, vacuum robot cleaner, and high-performance computing terminals. By providing a silicon-proven foundation, the platform enables our customers to accelerate time-to-market while significantly mitigating the engineering risks typically associated with high-end custom SoC development.

Data centers devices

Intelligent cockpit

Industrial human-machine interaction

Wearable

Transcoding SoC Platform

Built on our High-Performance SoC Platform, our Transcoding SoC Platform is a high-concurrency, heterogeneous computing architecture designed specifically for data centers. It addresses the growing computational demands arising from large-scale video streaming and AIGC applications.

This platform integrates our proprietary VPU IP with advanced pixel-processing technologies, including super-resolution. It is engineered to deliver high-quality video output while optimizing power consumption and reducing latency per channel, thereby helping CSPs lower the total cost of server operations.

As of December 31, 2025, we have deployed two generations of this transcoding SoC architecture on 14nm and 5nm process nodes. We provide comprehensive custom silicon solution service, enabling the simultaneous encoding and decoding of up to 32 high-definition video streams. These solutions have been adopted by seven of the global top 20 CSPs and three of the top five Internet companies in China. A next-generation, AI-enhanced transcoding platform on advanced process nodes is under development as of December 31, 2025.

Video streaming
Security

Remote healthcare and education

Security

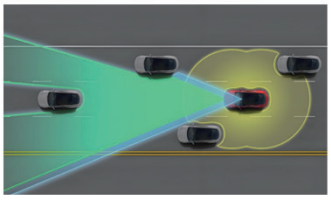
Gaming

Autonomous Driving SoC Platform

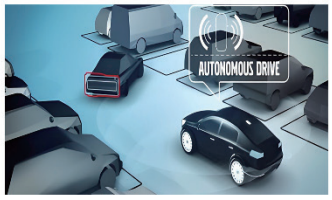
As another platform derived from our High-Performance SoC Platform, our autonomous driving SoC platform features a high-performance network-on-chip, CPUs and NPUs. It integrates our ASIL D-compliant functional-safety island IP, supporting customers' products in achieving ISO 26262 certification.

As a core component of the autonomous driving platform, we have developed a full spectrum of IPs to meet diverse functional-safety requirements across different automotive safety integrity levels. In addition to the autonomous driving platform, we also provide software design service to support customers in bringing vehicles into commercialization and mass production stage.

This platform has been successfully deployed in customer projects based on the 5nm advanced process node. The next-generation autonomous driving platform is currently being designed for deployment on more advanced process nodes, with enhanced connectivity and bandwidth supported by PCIe and UCIe interfaces.



Highway Autopilot



Autonomous Valet Parking

RoboTaxi

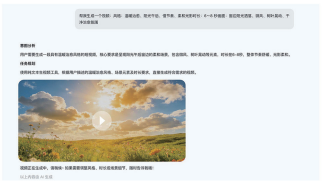
High-performance AIGC Platform

Our High-Performance AIGC Platform adopts an advanced custom silicon architecture engineered to support AIGC workloads. This platform integrates a comprehensive suite of computing technologies, including GPGPUs, NPUs and other specialized processing units, to deliver optimized AI performance.

This architecture incorporates a range of high-bandwidth memory solutions, such as LPDDR6, LPDDR5x and high bandwidth memory and features high-speed interconnects including PCIe 5.0, 56G/112G SerDes and UCIe, to support efficient data transfer and scalability within complex AIGC systems. We also provide a Linux-based software development kit tailored for customer-specific AIGC SoCs to support customers' training and inference requirements.

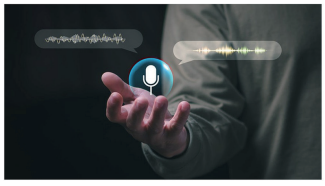
This platform has been deployed across multiple customer projects using advanced process nodes. As of the Latest Practicable Date, one AI ASIC has already been successfully taped out.

Image generation



Video generation

Text creation



Music creation

Financial analysis

Personalized education

AI Image Signal Processing ("AI-ISP") SoC Platform

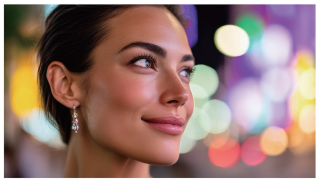
By integrating full-stack SoC RTL, back-end physical design and a real-time software SDK, our AI-ISP SoC Platform provides customers with a comprehensive custom silicon solution. This integrated approach supports chip development from the underlying silicon architecture to upper-layer algorithm implementation.

This platform architecture features a dedicated NPU and an image pre-processing unit. Utilizing our proprietary FLEXA synchronous interface technology, it achieves a low-power, low-latency and DDR-less design. This configuration mitigates legacy systems' image-processing bandwidth constraints and enables AI-driven image quality enhancement and adaptive computing under strict power requirements.

As of December 31, 2025, this solution has been adopted by internationally renowned smartphone brands and in mass production.

Ultimate night photography

Scene recognition and optimization



Smart portrait and video bokeh

AI super resolution

Background processing

Video stabilization and motion compensation

Ultra-low-energy AI/AR Glasses SoC Platform

Given the diversity of the AI/AR glasses market, our ultra-low-energy AI/AR Glasses SoC Platform provides a flexible and configurable custom architecture designed to meet the requirements of different market segments. It supports various camera configurations, multiple output interfaces and optional connectivity solutions.

To address the strict wearability constraints of AR devices, the platform adopts a dual-chip distributed architecture and advanced HB-PoP packaging technology. Its hardware features include control of up to 22 independent power domains, a DDR-less operating mode and a multi-level standby system with voice and video wake-up, which together help to minimize power consumption and thermal output. In addition, we also design dedicated micro LED driver and video processing chip for our customers to interface with various display technologies.

By integrating these technologies, we have built a complete custom ASIC platform to support spatial computing applications in the emerging AI/AR market. As of December 31, 2025, this platform has been used to develop AI/AR chips for a leading global Internet company, supporting the commercialization of next-generation wearable devices.

Entry-level

Mid-range

High-end

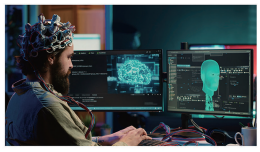
Mixed-signal ASIC Platform

Leveraging our infrastructure IPs and low-power mixed-signal IPs, we have developed a proprietary mixed-signal ASIC platform to support the design of custom ASICs for a wide range of applications.

As of December 31, 2025, this platform has been deployed in multiple customer projects, including applications such as home security cameras, on-board diagnostics systems and BLE MCUs.

By integrating a comprehensive suite of mixed signal IPs, including power switches, ring oscillators, low dropout regulators, MIPI C/D PHY interfaces and 802.11ah RF/baseband connectivity, and leveraging our design service, a home security camera SoC developed on this platform has achieved significant market penetration, with cumulative shipments exceeding 120 million units as of December 31, 2025.

Automotive diagnostics



Brain-computer interface

Micro-LED driver

eMMC/SD controller

Low-Power BLE MCU Solution

With our full suite of mixed-signal IPs and a complete set of BLE IPs covering the RF, baseband and software stack, we have developed a BLE MCU solution based on the 22nm FD-SOI process node. This solution has been adopted by a global Tier-1 microcontroller company.

In addition, we provide customers with production-ready SDKs to enhance their product competitiveness and shorten time-to-market.

Smart Home

Wearables

Healthcare

Consumer Electronics

Industrial & IoT

Automotive

VeriHealthi Platform and Solutions

We are strategically expanding from traditional consumer electronics into the high-growth "Big Health" market. We have launched the "VeriHealthi" platform, which, anchored by our proprietary IPs, provides integrated health detection solutions spanning from custom silicon design to reference applications. Our VeriHealthi platform offers multiple levels of licensing and custom design service – including software SDKs, health algorithms and intelligent hardware thereby providing enterprise customers with diverse options and flexible configuration capabilities.

Based on this platform, we have delivered customized silicon designs for invasive brain-computer interface chips, capsule endoscopy chips and wearable low-power Bluetooth chips to multiple global clients. In addition, we have independently developed over 20 health algorithms covering electrocardiogram (ECG) measurements, blood pressure monitoring and blood glucose measurement. We will continuously iterate these core technologies to accelerate the commercialization of emerging health devices, such as AI rings, brain-computer interface health monitors and intelligent rehabilitation robots, thereby providing the underlying technical support for application scenarios including physical examinations, smart elderly care and medical rehabilitation.

Brain-computer interface

Capsule endoscopy

Health wearables

Digital human body

Smart elderly care

Sports monitoring

Our Technologies

We have developed a series of key technologies for our custom silicon solution services and semiconductor IP licensing service.

Technologies for Custom Silicon Solution Service

Architecture Evaluation Technology

Architecture evaluation refers to the process of performing both qualitative and quantitative evaluations at an early stage of design, based on application scenarios defined in accordance with product specifications. These evaluations cover the overall design architecture, key functional modules, IP performance metrics and design parameters and form the basis for defining chip architecture.

We leverage our accumulated design experience and established platform architectures, together with advanced EDA tools and our proprietary performance models for functional modules, and incorporate measured data from existing products, to significantly enhance the accuracy of early-stage architecture evaluation as compared to theoretical estimations. We have also applied our evaluation platform in our existing ASIC design service to complete architecture design. These capabilities enables us to avoid design rework or over-design arising from suboptimal architecture definition, thereby shortening design cycles.

Large-scale SoC Verification Technology

Design verification is an essential part of the chip design and implementation process to ensure the design quality and shorten the design cycle. As the design scale and design complexity of large-scale SoC have increased significantly, resulting in a significant increase in the difficulty of design verification, legacy verification methods may not be sufficient to meet the needs of design verification in certain projects.

Combining various verification methods such as ASIC simulation, FPGA platforms and hardware acceleration/emulator platforms, our large-scale SoC verification platform can support verification of SoCs with more than 1 billion logic gates, supporting the verification of complex application-processor-level SoCs. It also enables early development and verification of device drivers and SDKs, thereby meeting both the completeness and time-to-market requirements of design verification.

Design Techniques for Advanced Process Nodes

As manufacturing processes evolve, the complexity of the design process increases significantly. For different foundries and process nodes, it is generally necessary to define corresponding design processes and design methodologies and verify them through tape-outs.

Our design technology can support both mature CMOS 28nm and above process node, as well as advanced process nodes including FinFET at 14nm/10nm/7nm/6nm/5nm/4nm process nodes and FD-SOI at 28nm/22nm process nodes. In particular, we have implemented adaptive body-biasing technology on the FD-SOI 22nm process node, which delivers significant benefits for ultra-low-energy IoT applications.

Design Process Construction in Accordance with the ISO 26262 Standard

We have established a design process construction that complies with the ISO 26262 standard and obtained certification from TÜV Rheinland, an independent international testing, inspection and certification organization. With this certifications, we can follow internationally recognized functional-safety design processes for automotive chips and provide design service that meet various automotive safety integrity levels for our customers.

Platform-Based Software Development Technology

To meet the needs of different customers and markets, we have designed and developed tiered, modular and reusable driver software and middleware development kits for different types of high-performance application processors, SoCs and microcontrollers. These kits are based on mainstream operating systems, which are able to meet the needs of various products including notebook computers, media player boxes, IoT, wireless Bluetooth headsets and other wearable devices.

We have designed Linux SDKs and Chromium OS and Android system SDKs for application processors, and have also designed IoT system software platforms for low-power SoCs and MCUs based on FreeRTOS, which can help customers quickly develop application software and shorten the volume production cycles for their products.

Technologies for IP Licensing Service

Our IP constitutes the core of our technologies and forms the basis of our IP licensing service, enabling us to deliver our customers scalable and differentiated services. See " — Our IP and IP Platform."

R&D Centers and Personnel

As of December 31, 2025, we have established R&D centers in nine cities (including locations in the PRC and overseas), which allows us to incorporate newly developed and leading technologies into our R&D projects. As of December 31, 2025, we had 1,839 employees dedicated to R&D, representing approximately 89.4% of our total number of employees. Our R&D team includes engineers with experience in the semiconductor industry. As of December 31, 2025, approximately 88.4% of our R&D employees held a master's or doctorate degree.

R&D Expenses

In 2023, 2024 and 2025, our R&D expenses amounted to RMB947.2 million, RMB1,247.3 million and RMB1,312.7 million, respectively, representing 40.7%, 53.8% and 41.7% of our revenue for the same respective years.

SALES AND MARKETING

We have established a global sales and marketing platform to support our business growth and deepen our engagement with key customers. We maintain sales and technical support teams in a number of locations in which our major customers are located, including China, the United States, Europe, Japan and South Korea. This network enables us to closely monitor market developments and customer requirements and effectively promote and deliver our services across our target markets.

Our regional sales teams work in close coordination with our technical support team to provide customers with timely and localized support. Through this integrated sales and technical support model, we aim to improve our responsiveness to customer requests, enhance customer satisfaction and foster long-term, strategic relationships with leading industry participants in our key markets.

Our Customers

Our customers primarily consist of chip companies (including fabless companies and IDMs) and system vendors (including Internet companies, CSPs, automotive companies and other OEMs). As of December 31, 2025, we had served approximately 350 customers for our custom silicon solution service and more than 465 customers for our IP licensing service.

In 2023, 2024 and 2025, sales to our five largest customers amounted to RMB1,086.7 million, RMB1,033.0 million and RMB1,434.3 million, respectively, accounting for 46.7%, 44.6% and 45.6% of our total revenue in these respective years. In 2023, 2024 and 2025, sales to our largest customer amounted to RMB535.1 million, RMB469.2 million and RMB503.9 million, respectively, accounting for 23.0%, 20.3% and 16.0% of our total revenue in these respective years. During the Track Record Period, to the best knowledge of our Directors, none of our Directors, their associates or any of our current Shareholders (who, to the knowledge of our Directors, own more than 5% of our share capital) had any interest in our five largest customers in any period during the Track Record Period that are required to be disclosed under the Hong Kong Listing Rules.

For the year ended December 31, 2025

	Customer	Revenue	Percentage of revenue	Year of commencement of business relationship	Major services provided	Credit terms	Background
		(in RMB thousands)	*%*				
1	Customer A . . .	503,934	16.0	2018	Custom silicon solution service and IP licensing service	Mainly 90 days after the invoice date	Customer A is a US-listed multinational technology company, engaged in e-commerce, cloud computing, online advertising, digital streaming, and artificial AI, headquartered in the United States.
2	Customer B . . .	486,636	15.5	2023	Custom silicon solution service and IP licensing service	Mainly 30 days after the invocie date	Customer B is a private company engaged in the fields of electronic components and IC design, headquartered in China.
3	Customer C . . .	182,774	5.8	2019	Custom silicon solution service and IP licensing service	Mainly 5 working days after the invoice date	Customer C is a private company engaged in IC design for industrial and consumer electronics, headquartered in China.
4	Customer D . . .	153,492	4.9	2023	Custom silicon solution service and IP licensing service	Mainly 30 working days after the invoice date	Customer D is a private technology company that designs and develops smartphones, smartphone accessories, software and online services, headquartered in China.
5	Customer E . . .	107,505	3.4	2025	Custom silicon solution service and IP licensing service	30 days after the invoice date	Customer E is a private Internet company engaged in cloud and industrial service, headquartered in China.

For the year ended December 31, 2024

	Customer	Revenue	Percentage of revenue	Year of commencement of business relationship	Major services provided	Credit terms	Background
		(in RMB thousands)	*%*				
1	Customer A . . .	469,231	20.3	2018	Custom silicon solution service and IP licensing service	Mainly 90 days after the invoice date	Customer A is a US-listed multinational technology company, engaged in e-commerce, cloud computing, online advertising, digital streaming, and artificial AI, headquartered in the United States.
2	Customer F . . .	205,022	8.8	2022	Custom silicon solution service and IP licensing service	Mainly 7 days after the invoice date	Customer F is a private company engaged in IC chip design and related services, headquartered in China.
3	Customer B . . .	157,355	6.8	2023	Custom silicon solution service and IP licensing service	Mainly 30 days after the invoice date	Customer B is a private company engaged in the fields of electronic components and IC design, headquartered in China.
4	Customer G . . .	101,051	4.4	2023	Custom silicon solution service and IP licensing service	Mainly 30 days after the invoice date	Customer G is a company engaged in automotive technology, software, big data and charging services, headquartered in China. Customer G is a subsidiary of a dual-listed Company.
5	Customer D . . .	100,346	4.3	2023	Custom silicon solution service	Mainly 30 working days after the invoice date	Customer D is a private technology company that designs and develops smartphones, smartphone accessories, software and online services, headquartered in China.

For the year ended December 31, 2023

	Customer	Revenue	Percentage of revenue	Year of commencement of business relationship	Major services provided	Credit terms	Background
		(in RMB thousands)	*%*				
1	Customer A . . .	535,081	23.0	2018	Custom silicon solution service and IP licensing service	Mainly 90 days after the invoice date	Customer A is a US-listed multinational technology company, engaged in e-commerce, cloud computing, online advertising, digital streaming, and artificial AI, headquartered in the United States.
2	Customer H . . .	270,160	11.6	2016	Custom silicon solution service and IP licensing service	Mainly 10% payable in advance and 90% payable within 10 days	Customer H is a company engaged in the R&D, production, sales and technical services of intelligent products in the fields of electric power and fire electronic alarm systems, headquartered in China. Its shares are listed in China.
3	Customer B . . .	125,416	5.4	2023	IP licensing service	Mainly 30 days after the invoice date	Customer B is a private company engaged in the fields of electronic components and the IC design, headquartered in China.
4	Customer I. . . .	78,433	3.4	2019	Custom silicon solution service and IP licensing service	Mainly open account 30 days	Customer I is an integrator, trade, distributor and supplier of technology solution, headquartered in Japan. Shares of its parent company are listed in Japan.
5	Customer J . . .	77,605	3.3	2012	Custom silicon solution service and IP licensing service	Mainly 60 days after the invoice date	Customer J is a company specializing in designing and manufacturing high-performance mixed-signal and microcontroller semiconductor products, headquartered in the United States. Customer J is a subsidiary of a US-listed Company.

Pricing

In determining the pricing of our solutions, we take into account factors such as the type of services involved, the level of market competition, the customer's industry position, transaction scale and amount and whether the project involves leading technologies within its relevant niche segment. The final pricing is determined through negotiations with the customer.

Arrangement with Our Customers

We typically enter into framework agreements with our major customers, with actual prices and volumes specified in individual purchase orders. The terms of these agreements vary depending on the specific service or project and the result of our negotiation with each customer, but these agreements generally contain the following terms:

Price	:	Pricing of the services is generally specified in the respective purchase order or agreement
Scope of service	:	Scope of service is set forth in the respective agreement
Payment and credit terms	:	Payment is generally made in accordance with agreed payment schedules in accordance with the type of service.
Minimum purchase requirements	:	Our framework agreements generally do not contain minimum purchase requirements.
Confidentiality	:	These framework agreements usually have strict confidentiality provisions.
Termination and renewal	:	These framework agreements can be terminated with mutual agreement by parties.

SEASONALITY

Demand for and sales of our services are linked to the seasonality of their respective end products and markets. Revenue in the second half of each year is typically higher than the first half, largely reflecting increased demand from certain customers in connection with year-end holiday sales, in particular customers in the consumer electronics sector. For further details on risks associated with seasonality. See "Risk Factors – Our sales may be influenced by seasonality."

OPERATIONS AND SUPPLY CHAIN

Supply Chain and Procurement

We have established a comprehensive and stable procurement management process and use SAP, an enterprise resource planning system, as our primary tool to execute and manage our procurement activities. Our procurement model primarily consists of (i) a general procurement model and (ii) a customer order-driven procurement model.

Our general procurement model mainly applies to the purchase of standard software and hardware. The principal categories of items we procure under this model include EDA and design tools, verification tools, laboratory and test equipment, servers, and storage equipment.

Our customer order-driven procurement model mainly applies to our chip customization services. Based on our customers' mass production chip orders, we procure wafers from foundries and packaging and testing services from packaging and testing service providers on an outsourced basis in order to complete the manufacturing of chips.

Our Suppliers

Our major suppliers primarily consist of wafer foundries, OSAT partners and IP/EDA suppliers. We have established and maintain stable and long-term relationships with these major suppliers.

Selection and Management of Suppliers

We have established and implemented a supplier selection and management framework. In selecting suppliers, we take into account a range of factors, including their industry position, technical capabilities, product and service quality, pricing and payment terms. We also adopt a foundry-neutral strategy, which allows us to manage our supply chain flexibly across multiple suppliers, diversify supply risks and enhance our overall resilience.

Major Suppliers

In 2023, 2024 and 2025, purchases from our five largest suppliers amounted to RMB656.7 million, RMB803.8 million and RMB1,297.6 million, respectively, accounting for 73.6%, 67.2% and 67.7% of our total purchases in these respective years. In 2023, 2024 and 2025, purchases from our largest supplier amounted to RMB264.3 million, RMB213.8 million and RMB546.1 million, respectively, accounting for 29.6%, 17.9% and 28.5% of our total purchases in these respective years. During the Track Record Period, to the best knowledge of our Directors, none of our Directors, their associates or any of our current Shareholders (who, to the knowledge of our Directors, own more than 5% of our share capital) had any interest in our five largest suppliers in any period during the Track Record Period that are required to be disclosed under the Listing Rules.

For the year ended December 31, 2025

	Supplier	Purchase amount	Percentage of procurement	Year of Commencement of business relationship	Type of purchase	Credit terms	Background
		(in RMB thousands)	*%*				
1	Supplier A	546,081	28.5	2020	Wafer	60 days after the invoice date	Supplier A is a private company, headquartered in China that engages in the distribution of electronic components and a distributor of Supplier F.
2	Supplier B	321,227	16.8	2011	Wafer	30 days after the invoice date	Supplier B is a US-listed multinational semiconductor manufacturing company, headquartered in the United States.
3	Supplier C	175,921	9.2	2007	Wafer	Mainly prepayment	Supplier C is a US-listed, global leading semiconductor manufacturing company, headquartered in Taiwan.
4	Supplier D	131,506	6.9	2006	Wafer	30 days after the invoice date	Supplier D is an A-Share-listed semiconductor manufacturing company, headquartered in China.
5	Supplier E	122,882	6.4	2025	IP/EDA	5 days after the invoice date	Supplier E is a private provider of chip design and IP solution, headquartered in Singapore.

For the year ended December 31, 2024

	Supplier	Purchase amount	Percentage of procurement	Year of Commencement of business relationship	Type of Purchase	Credit terms	Background
		(in RMB thousands)	*%*				
1	Supplier B	213,777	17.9	2011	Wafer	30 days after the invoice date	Supplier B is a US-listed multinational semiconductor manufacturing company, headquartered in the United States.
2	Supplier D	165,396	13.8	2006	Wafer	30 days after the invoice date	Supplier D is an A-Share-listed semiconductor manufacturing company, headquartered in China.
3	Supplier A	149,293	12.5	2020	Wafer	60 days after the invoice date	Supplier A is a private company, headquartered in China that engages in the distribution of electronic components and a distributor of Supplier F.
4	Supplier F	139,482	11.7	2014	Wafer	60 days after the invoice date	Supplier F is a Korean-listed multinational manufacturer of consumer and industrial electronic equipment and products, headquartered in South Korea.
5	Supplier G	135,847	11.4	2003	IP/EDA	30 days after the invoice date	Supplier G is a US-listed global leading provider of EDA tools and semiconductor IP, headquartered in the United States.

the year ended December 31, 2023

	Supplier	Purchase amount	Percentage of procurement	Year of Commencement of business relationship	Type of Purchase	Credit terms	Background
		(in RMB thousands)	*%*				
1	Supplier B	264,307	29.6	2011	Wafer	30 days after the invoice date	Supplier B is a US-listed multinational semiconductor manufacturing company, headquartered in the United States.
2	Supplier C	129,284	14.5	2006	Wafer	Mainly prepayment	Supplier C is a US-listed, global leading semiconductor manufacturing company, headquartered in Taiwan.
3	Supplier H	109,285	12.2	2011	Packaging and testing	30 days after the invoice date	Supplier H is an A-Share-listed multinational manufacturing company of semiconductor packaging and testing services, headquartered in China.
4	Supplier I.	89,552	10.0	2020	IP/EDA	30 days after the invoice date	Supplier I is a UK-listed leading provider of high-speed interface semiconductor IP solution, headquartered in Canada.
5	Supplier A	64,310	7.2	2020	Wafer	60 days	Supplier A is a private company, headquartered in China that engages in the distribution of electronic components and a distributor of Supplier F.

Arrangement with our Suppliers

Key Terms of Our Agreements with Suppliers

The terms of these agreements vary by service or project and may be affected by a range of factors, including, among others, the foundry's available capacity, but generally include the following provisions:

Price	:	Pricing of the chips and testing are generally specified in purchase orders
Scope and specifications	:	The framework agreements typically set out the general scope and categories of products and services to be provided, while detailed specifications, quality requirements and delivery schedules are agreed in individual purchase orders or separate technical documents.
Quality	:	We generally require suppliers to comply with agreed quality standards and applicable industry norms. Suppliers are typically responsible for conducting necessary inspections and tests to ensure that their products and services meet contractual requirements.
Pricing and payment terms:	:	Pricing is usually determined based on product type, process or service scope and is specified in the relevant purchase orders or project agreements. Payment is generally made in accordance with agreed payment terms, which may take into account project milestones, delivery timing and credit arrangements.
Confidentiality	:	These framework agreements usually have strict confidentiality provisions.
Termination	:	These framework agreements are generally entered into for a fixed term and may be terminated by either party in accordance with the termination provisions agreed between the parties, including termination by mutual consent and termination upon the occurrence of specified events or breaches.

During the Track Record Period and up to the Latest Practicable Date, we did not experience any material breaches by our suppliers.

Suppliers-Customers Overlap

Supplier F was one of our top five suppliers in 2024. Our procurement from Supplier F amounted to RMB139.5 million, accounting for 11.7% of our total procurement amount in the same year. Our revenue from Supplier F amounted to RMB1.8 million, accounting for 0.1% of our total revenue in the same year. We mostly purchased wafers from Supplier F while we provide IP licensing service to Supplier F.

Supplier D was one of our top five suppliers in 2023, 2024 and 2025. Our procurement from Supplier D amounted to RMB129.3 million, RMB165.4 million and RMB131.5 million, accounting for 14.5%, 13.8% and 6.9%, respectively. Our revenue from Supplier D amounted to RMB3.6 million, RMB3.0 million and RMB3.4 million, accounting for 0.2%, 0.1% and 0.1% in 2023, 2024 and 2025, respectively. We mostly purchased wafer from Supplier D while we receive IP royalties from Supplier D.

Save as disclosed above, none of our Group's five largest suppliers in 2023, 2024 or 2025 were also our Group's customers in the same year and none of our five largest customers in

2023, 2024 and 2025 were also our suppliers in the same years, respectively. In addition, from a business perspective, the transactions that we entered into with the overlapping supplier-customers were on an arm's length, mutually independent basis under normal commercial terms. Negotiations of the terms of our sales to and purchases from these overlapping supplier-customers were conducted on an individual basis, undertaken by different departments and entities both in our Group and in the overlapping supplier-customers, and the sales and purchases were neither inter-connected nor inter-conditional with each other.

For the overlapping supplier-customer, the key terms of our sales and supply agreements were substantially similar to those of our other customers/suppliers. According to CIC, it is consistent with industry practice for a company to have both sales to and purchases from the same or related customer/supplier.

Inventory Management

Our inventories mainly comprise work-in-progress and finished goods. Under our SiPaaS model, we do not sell chip products and generally do not hold substantial inventories of finished products for sale, which reduces our exposure to market and inventory risks compared with legacy fabless companies. We generally arrange procurement and outsourced production based on customers' purchase orders and forecasts. Our operations team reviews inventory levels on a regular basis, taking into account customers' project schedules and demand forecasts and adjusts our procurement and production plans accordingly. We also monitor inventory aging with a view to managing the risk of inventory obsolescence.

As of December 31, 2023, 2024 and 2025, our inventories amounted to RMB278.6 million, RMB395.5 million and RMB498.0 million, and our inventory turnover days in 2023, 2024 and 2025 were 179 days, 195 days and 162 days.

Quality Control

We believe that quality is essential to our business operations and sustainable growth. We are committed to delivering services that meet the highest industry standards and exceed customer expectations. Our comprehensive quality control and quality assurance systems are integrated into every stage of our service process, ensuring consistent and reliable delivery of high-quality services.

We have established an ISO 9001-certified quality management system. We conduct regular internal audits and management reviews of our quality control systems to promptly identify and address potential issues, ensuring continuous improvement and refinement of our quality control systems.

INTELLECTUAL PROPERTY

As of December 31, 2025, our research and development efforts have produced 240 invention patents, three utility model patents, two design patents, 12 software copyrights, 151 registered trademarks, 273 registered IC layout-design rights. See "Appendix VI – Statutory and General Information – Further Information about the Business – Intellectual Property."

We rely on a combination of intellectual property protection laws and contractual arrangements (including confidentiality provisions) to establish and protect our proprietary technologies, know-how and other intellectual property rights. We proactively manage and expand our intellectual property portfolio and use confidentiality and non-compete agreements to protect our intellectual property and trade secrets. Despite our efforts, we may be subject to risks associated with alleged infringement of third parties' intellectual property rights, or infringement of our intellectual property rights by third parties. See "Risk Factors – Risks Relating to Our Business — We may not be able to adequately protect our IP rights, which could materially and adversely affect our business, financial condition, and results of operations."

During the Track Record Period, we did not experience any material infringement of our intellectual property rights.

DATA PRIVACY AND CYBERSECURITY

In recent years, data privacy and cybersecurity have emerged as critical governance priorities for companies worldwide. In particular, the PRC legislative and government authorities regularly introduce new cybersecurity, data security and privacy laws and regulations. Consequently, our practices regarding the collection, process and transfer of various types of data may come under increased administrative scrutiny.

We collect and store data generated during or in connection with our business operations, including data related to our business and transactions with our customers, and suppliers. As our customers are brand companies rather than individuals, we only involve in personal information collection during our business operations in very limited circumstances and we do not actively process such personal information. In addition, we are not an operator of a critical information infrastructure recognized by the Cyberspace Administration of China, the MIIT or other relevant PRC governmental authorities.

We have established comprehensive internal policies in relation to network security and data compliance. Our data security policies have been certified under ISO 27001:2013. We emphasize the importance of information security to our employees through meetings and special trainings and ensure our employees have a good understanding of our information security management system.

We have established information technology department responsible for network data and information protection and we have appointed specific persons in charge of network security and of data security.

During the Track Record Period and up to the Latest Practicable Date, we have not received any claim from any third party against us on the ground of infringement of such party's right to data and privacy protection as provided by any applicable laws and regulations.

INFORMATION TECHNOLOGY

Our information technology department is responsible for developing and maintaining information technology systems to support our business operations and growth.

The capabilities and the stability of our IT infrastructure are vital to our business operations. Our IT department performs system checks, data back-ups, system maintenance and other activities to secure the continual operation of our critical IT systems and facilities. During the Track Record Period and up to the Latest Practicable Date, we did not experience any material failure or general breakdown of our IT systems which resulted in a material adverse impact on our overall business operations.

PROPERTIES

As of December 31, 2025, we operated our business through three owned properties and 18 leased properties in China. We primarily use our owned and leased properties as our R&D centers, sales support centers and office premises.

As of December 31, 2025, we had no single property with a carrying amount of 15% or more of our total assets, and on this basis, we are not required by Rule 5.01A of the Listing Rules to include any valuation report in this document. Pursuant to section 6(2) of the Companies Ordinance (Exemption of Companies and Prospectuses from Compliance with Provisions) Notice, this document is exempted from compliance with the requirements of section 342(1)(b) of the Companies (Winding Up and Miscellaneous Provisions) Ordinance in relation to paragraph 34(2) of the Third Schedule to the Companies (Winding Up and Miscellaneous Provisions) Ordinance, which requires a valuation report with respect to all of our interests in land or buildings.

Owned Properties

As of December 31, 2025, we owned three land use rights and 18 properties with a gross floor area of 30,016.1 sq.m. in Chinese mainland. We mainly use these properties as our R&D centers and sales support centers.

Leased Properties

As of December 31, 2025, we leased 29 properties, of which 18 properties with an aggregate gross floor area of 31,962.9 sq.m. were located in Chinese mainland, and eight properties were located in Hong Kong, the United States, France, Japan and Vietnam, mainly as our office premises.

EMPLOYEES

We believe that our long-term growth depends on the expertise, experience and development of our employees. As of December 31, 2025, we had 2,057 full-time employees. Substantially all of our employees were in China. The following table sets forth a breakdown of our full-time employees by function as of December 31, 2025.

Function	As of December 31, 2025	
	Number	*%*
R&D	1,839	89.4
Management and Administration	156	7.6
Sales	36	1.8
Operations	26	1.3
Total	**2,057**	**100.0**

Our workforce comprises highly skilled workers and professionals, many of whom have extensive knowledge and experience in the semiconductor business. As of December 31, 2025, our employees in Chinese mainland with more than 10 years of work experience accounted for 25.0% of our workforce and our employees have an average age of approximately 32.

We provide our employees with certain benefits including social insurance coverage and retirement benefits. We enter into individual employment contracts with our employees to cover matters such as wages, employee benefits, confidentiality and grounds for termination. Our employees' compensation is determined with reference to their job positions, technical skills, job performance and competition. We have various employee training programs that aim to enhance our employees' technical skills and innovation capability.

Our Directors consider that our Group has maintained a good relationship with our employees. During the Track Record Period, there was no material dispute between our Group and our employees, and we did not experience any strikes, work stoppages, labor disputes or actions which had a material adverse effect on our business and operations.

COMPETITION

The markets for our services are highly competitive and are characterized by rapid technological change, evolving industry standards and changing customer requirements. Our customers and potential customers also seek to manage their overall cost of design and may consolidate their procurement with a limited number of vendors. We compete with other providers of semiconductor IP and design services, as well as with in-house engineering teams of semiconductor companies that develop IP or undertake design work internally. As the markets in which we operate continue to develop, we expect existing competitors to increase their investments and new market participants to emerge. See "Industry Overview" for details relating to our competitive landscape.

AWARDS AND RECOGNITION

The following table sets out a summary of the major awards and recognitions we received during the Track Record Period and up to December 31, 2025.

No.	Year	Awards or Recognition
1	2024	China IC Design Achievement Award — "IP Company of the Year for Outstanding Industry Impact"
2	2024	China IC Design Achievement Award — "Outstanding IC Design Service Company of the Year"
3	2025	Nominee for National Intellectual Property Model Enterprise
4	2025	The Most Innovative Sci-Tech Innovation Board Listed Companies
5	2025	China IC Design Achievement Award — "IC Design Service Company of the Year for Outstanding Performance"

INSURANCE

We review our insurance policies from time to time to assess the adequacy and breadth of coverage. We believe that our existing insurance coverage is adequate for our business operations and is in line with industry standards in the countries in which we operate. Nevertheless, we may be exposed to claims and liabilities which exceed our insurance coverage.

During the Track Record Period, we did not make, and were not the subject of, any insurance claims which are material to our business or financial condition.

RISK MANAGEMENT AND INTERNAL CONTROL

Our future operating performance may be affected by risks relating to our business. Some of these risks are specific to us while others relate to economic conditions and the general industry in which we operate. See "Risk Factors" for a discussion of these risks.

The Board of Directors and our senior management are responsible for establishing and maintaining adequate risk management and internal control systems. Risk management is the process designed to identify potential events that may affect us and to manage risks to be within our risk appetite. Internal control is the process designed to provide reasonable assurance regarding achievement of objectives related to effectiveness and efficiency of operations, reliability of financial reporting and compliance with applicable laws and regulations.

Risk Management and Internal Control Policies

We have implemented or will adopt upon [**REDACTED**] a number of policies and measures to manage our risks and set up proper internal controls. These policies cover areas such as (i) the duties and roles of the Directors, the Board and our senior management; (ii) social and environmental matters, including policies on diversity; (iii) financial reporting; (iv) whistleblowing; (v) prevention of market misconduct, (vi) anti-corruption and anti-bribery, (vii) export control compliance and (viii) compliance with the Listing Rules.

Under our risk management and internal control policies, the Board oversees risk management and internal control systems on an ongoing basis and reviews the effectiveness of these systems. In particular, we have adopted anti-corruption and anti-bribery policies under which all employees are required to comply with applicable laws and internal guidelines, refrain from any conduct that may give rise to bribery or corruption risks and promptly report any actual or suspected violations through established reporting channels. We also provide regular anti-corruption training to employees.

We have also implemented an export control internal compliance program to ensure compliance with applicable export control laws and regulations in the jurisdictions in which we operate. This program includes the classification of products under relevant regulations, assessment of end use and end users and screening of counterparties involved in each transaction.

In February 2026, we engaged an independent consulting firm to perform a general review over our internal controls. The key areas of inspection include financial reporting and disclosure, research and development management, management policies over sales, supply chain controls, trade receivables and payables management, and delivery control, inventory management, intangible assets management, human resource and remuneration management, capital management, tax management, insurance management, contract control and information system control.

LICENSES, PERMITS AND APPROVALS

We are required to obtain or maintain various licenses, permits and approvals in order to operate our business. We believe we have all material licenses, permits and approvals necessary in order to operate our business. We continually monitor our compliance with these requirements in order to ensure that we have all such approvals, licenses and permits as are necessary to operate our business.

We had not experienced any material difficulties in renewing material licenses, permits or approvals during the Track Record Period and do not expect there to be any material difficulties in renewing them upon their expiry.

LEGAL PROCEEDINGS

We may from time to time become a party to various legal, arbitral or administrative proceedings arising in the ordinary course of our business. As of the Latest Practicable Date, there was no litigation, arbitration or administrative proceedings pending or threatened against us or any of our Directors which could have a material and adverse effect on our financial condition or results of operations.

During the Track Record Period and up to the Latest Practicable Date, there were no material breaches or violations of laws or regulations applicable to us which are expected to have a material adverse effect on our business, financial condition or results of operations.

ENVIRONMENT, SOCIAL REPONSIBILITIES AND GOVERNANCE

We put high emphasis on environmental and social matters, and have incorporated measures to address these matters into daily operations. By benchmarking to ESG topics listed in the Environmental, Social and Governance Reporting Code, sector guidance of International Sustainability Disclosure Guide and ESG disclosure made by listed companies in our sector, we have identified ESG topics highly material to our Group, including corporate governance, supply chain management, climate strategy, product liability, and employee management, and we have formed relevant policies, management process or operating manual, and have been monitoring the implementation of these policies during daily operation to promote the sustainable development of our Group.

ESG Governance

We have established an ESG governance structure: a Strategy and ESG Committee that operates under the Board of Directors and a cross-departmental ESG Working Group has been formed within management.

Our Strategy and ESG Committee is chaired by the Chairman, and members are our Directors. Committee's responsibilities include:

- advise the Board on ESG objectives, strategies, targets and guidelines.
- supervise, review and assess our Group's ESG implementation.
- review ESG reports and provide performance feedback to the Board.

Our ESG Working Group includes representatives from Board Office, HR & Admin, Legal, Finance, MarCom, Business Development (including Procurement and Quality Assurance), IT, IP Division, Custom Silicon Platform Division, Government Relations (including Intellectual Property). The responsibilities of the ESG Working Group include:

- track ESG laws, listing rules and policy updates.
- identify key stakeholders and respond to ESG concerns.
- conduct ESG risk assessment and management within functions.
- formulate ESG principles, strategies, materiality assessments and targets.
- evaluate and implement ESG policies, and report effectiveness to the ESG Committee.
- prepare external ESG disclosures and monitor major ESG risks.

Environmental

Use of Resources

In our owned or leased office spaces we incorporate energy conservation and emissions reduction, material consumption based on actual needs, and resource efficiency into all renovations and refurbishments. Notably, our office in Lingang in Shanghai's Pudong district represents the underlying asset for the nation's first green bond issuance backed by a green-certified building. We display energy-saving and water conservation posters throughout our offices to encourage eco-friendly workplace practices.

The following table sets forth our energy usage during the Track Record Period:

		Year ended December 31,		
Metrics[(1)]	**Unit**	**2023**	**2024**	**2025**
Purchased electricity	Kilowatt hour (kWh)	2,648,186.7	3,389,193.0	3,877,291.9
Natural gas	Cubic meter	12,712.7	5,003.8	11,836.9
Total comprehensive energy consumption *(Note 1)*	Megawatt hour (MWh)	2,785.8	3,443.3	4,005.4
Comprehensive energy consumption intensity	MWh/million revenue in RMB	1.2	1.5	1.3

Note:

(1) Comprehensive energy consumption refers to the "General Rules for Calculation of Comprehensive Energy Consumption" (GB/T 2589-2020) issued by the State Administration for Market Regulation and the National Standardization Administration.

For water resource management, we deploy water-saving equipment, enhance the maintenance inspections of water fixtures, and promote conservation awareness to minimize waste and improve recycling efficiency. The consumption of water resources (including pollution discharge fees) of our Group in 2023, 2024 and 2025 was RMB42,000, RMB51,000 and RMB56,000, respectively. Given the consumption levels, the impact of water resources use on our finance and operation is relatively low.

Waste management

Our waste includes end-of-life office electronics (e.g., computers, servers), hazardous waste (e.g., printer consumables), and non-hazardous waste (e.g., paper, plastics) from daily operations.

We strive for waste minimization and resource recovery through unified management of IT assets. This includes extending computer lifespans through upgrades and redistribution, repurposing servers, advancing paperless operations, establishing channels for idle item exchange, and setting up plastic bottle recycling points. Collected plastic bottles are regularly donated to partner organizations through the "Spring Rainfall Recycling Program."

For hazardous waste, we ensure precise sorting and secure interim storage, conduct routine inspections of dedicated storage areas to eliminate environmental and safety risks, and entrust all hazardous waste to certified professional entities for compliant, eco-friendly disposal. In 2023, 2024 and 2025, the total disposal expenses of hazardous waste of our Group were less than RMB10,000, and thus hazardous waste has a relatively low impact on our Group's finances and operations.

For non-hazardous waste, we continuously refine the classification and collection mechanisms to enhance the purity and value of recyclable materials. For recyclables such as cardboard boxes and plastics, we actively partner with recycling channels to boost recycling rates. The disposal expenses of non-hazardous waste of our Group were charged together with property service management fee in our financial reports, indicating that non-hazardous waste has no direct significant financial and operational impact on our Group.

Addressing climate change

Governance

In response to the challenge of global climate change, we proactively place climate change-related issues under the oversight of the Board of Directors. Concurrently, at the management level, our administration department oversees cross-departmental coordination and conducts regular assessments of climate-related risks. This approach is intended to ensure that all employees fully understand the current status and trends of these issues.

Strategy

Our Group actively pursues its "carbon peak and carbon neutrality" strategy in its daily operations. Through green office practices, energy-saving measures, environmental education programs, and the development of low-power chips, our Group promotes energy conservation and emissions reductions to contribute to global climate governance.

Risk Management

We proactively identify, assess, manage, and address climate change risks. For acute risks such as typhoons, earthquakes, extreme heat, and heavy rainfall, each local office has developed specific contingency plans, established dedicated emergency response teams, and conducted regular drills. This approach enhances our Group's preparedness and resilience to unforeseen events.

Metrics and Targets

To oversee and manage environmental indicators more efficiently, we regularly collect and conduct in-depth analyzes of relevant data. This provides a scientific basis for decision-making in our environmental protection efforts. We have consistently monitored key indicators closely linked to climate risks, such as direct GHG emissions (Scope 1) and indirect GHG emissions (Scope 2).

The following table sets forth our GHG emissions during the Track Record Period:

Metrics	Unit	Year ended December 31, 2023	2024	2025
Direct GHG emissions (Scope 1)[1]	Tons of CO2 equivalent	28.1	11.0	25.9
Indirect GHG emissions (Scope 2)[2]	Tons of CO2 equivalent	1,510.3	1,932.9	2,057.3
Total GHG emissions	Tons of CO2 equivalent	1,538.3	1,943.8	2,083.2
GHG emissions intensity	Kilogram CO2 equivalent/ revenue in million RMB	0.7	0.8	0.7

Notes:

(1) Direct GHG emissions (Scope 1) factor comes from China Energy Statistical Yearbook and IPCC 2006.

(2) Indirect GHG emissions (Scope 2) are calculated based on electricity consumption and emission factors, and the emission factors refer to the Notice of the Ministry of Ecology and Environment on Doing a Good Job in the Management of Greenhouse Gas Emission Reports of Power Generation Industry Enterprises from 2023 to 2025.

Society

Employment management and employee care

We are committed to ensuring fair and equitable treatment of all employees throughout recruitment and employment. We strictly prohibit discrimination based on nationality, race, ethnicity, gender, age, or any other factors. Furthermore, we forbid child labor, and oppose all forms of inhumane treatment, including sexual harassment, sexual abuse, corporal punishment, mental or physical coercion, and verbal abuse. To reinforce our stance against sexual harassment, we have distributed dedicated handbooks to all employees. During the Track Record Period, no incidents of employee discrimination, child labor, or forced labor were reported within our Group.

To deepen employees' sense of belonging and well-being, we conduct satisfaction surveys and implement a series of care and benefits initiatives. These include organizing family day events, summer camps, our anniversary celebrations, as well as hosting special gatherings such as the VeriSilicon Gala and Spring Festival Gala. Furthermore, our Group hosts diverse activities during important holidays such as Lantern Festival, Women's Day, Father's Day, Thanksgiving, and Dongzhi Festival to enrich our employees' lives and foster stronger bonds.

Training and development

We consistently value the growth and skill development of our employees. To this end, we have established a comprehensive, career-long training system that integrates online and offline learning. This system encompasses a wide range of training activities designed to effectively onboard new employees, enhance general competencies and professional expertise, cultivate management capabilities, and reinforce our core cultural values. These initiatives significantly boost employees' overall competency and professional skills while strengthening team cohesion and cultural identity.

Health and safety

We prioritize our employees' holistic well-being, connecting workplace safety with comprehensive health initiatives. Beyond creating a safe and healthy working environment, we actively promote physical and mental wellness. This approach includes providing annual health check-ups, comprehensive health insurance, mental health counseling services, strategically placed AEDs, and fully stocked first-aid kits. We also organize "Health Month" campaigns and conduct regular fire drills and first-aid training programs to continuously strengthen our employees' sense of security and health awareness.

Supply chain management

We have strengthened our supply chain management to mitigate relevant risks. Key actions we have implemented include defining clear supplier selection criteria, enhancing supplier risk management and oversight, establishing regular communication mechanisms, and empowering suppliers to grow. Collectively, these initiatives foster a sustainable supply chain. Upholding our fab-neutral strategy, we have integrated mineral sourcing responsibility clauses into our *Supplier Selection Procedures*.

Integrity and anti-corruption

We strictly comply with relevant anti-corruption laws and regulations such as the *Civil Code of the People's Republic of China* and the *Interim Provisions on Prohibition of Commercial Bribery*. Through our established *Code of Business Conduct for Employees*, we outline the core principles and rules governing employee conduct in both internal management and external business engagements. This framework helps ensure that all employees uphold business ethics and operate with integrity and fairness.

Corporate social responsibilities

Over the years, our Group has actively fulfilled its social responsibilities while driving its own business development. We proactively participate in public welfare activities in local communities. Key activities include joining Zhangjiang Science Hall Science Festival and hosting the Career Experience Summer Camp at Tianfu Software Park, fostering a harmonious relationship between our Group and our communities. Furthermore, through sustained efforts in educational assistance, we support disadvantaged groups, rural revitalization, and environmental protection, consistently demonstrating our commitment to corporate social responsibility.