# GLOSSARY OF TECHNICAL TERMS

***This glossary contains explanations of certain technical terms used in this document. As such, these terms and their meanings may not correspond to standard industry meanings or usage of these terms.***

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| "±" | symbol for "plus or minus" |
| "mΩ" | milliohm, a unit of electrical resistance |
| "μm" | micrometer |
| "1P1M" or "2P2M" or "3P3M" | "P" represents number of polyimide layers, "M" represents number of metal layers |
| "2.5D/3D" | packaging methods that connect multiple chips electrically through interposer (2.5D) or vertical stacking (3D) |
| "3D NAND" | three-dimensional NAND flash memory, a type of non-volatile storage technology where memory cells are stacked vertically in multiple layer |
| "3rd generation" | Stage 3 packaging and testing technologies covering QFN, BGA and WLP according to Frost & Sullivan |
| "4th generation" | Stage 4 packaging and testing technologies covering SiP and Bumping according to Frost & Sullivan |
| "5th generation" | Stage 5 packaging and testing technologies covering 2.5D/3D, TSV, Fan-Out among others, according to Frost & Sullivan process/packaging |
| "5G" | fifth generation of mobile network technology |
| "ANSI/ESD S20.20" | a standard developed by the American National Standards Institute and the Electrostatic Discharge Association for managing and mitigating the effects of electrostatic discharge on electronic devices |
| "ABF" | Ajinomoto Build-up Film, a high-performance insulating material used in semiconductor packaging |
| "AI" | artificial intelligence |
| "BGA" | Ball Grid Array |
| "Bins" | categories used to sort individual chip based on its performance and test results |
| "Bluetooth" | short-range wireless communication technology that allows devices to exchange data over radio waves |

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| "Bumping" | the process of creating solder balls or metal bumps on a chip's surface to enable electrical and mechanical connection to another substrate |
| "CAGR" | compound annual growth rate |
| "CAPiC" | Chiplet and Advanced Package integration Center |
| "chip" | a piece of silicon that contains integrated circuits used to perform electronic functions in devices |
| "chiplet" | a modular integrated circuit designed to be combined with other chiplets in a single package |
| "COWOS-S/L" | Chip-on-Wafer-on-Substrate (Silicon/Local Silicon Interconnect), a method that stacks chips on an interposer and substrate for high-performance packaging |
| "Cu" | a symbol for copper |
| "CPU" | central processing unit |
| "CPO" | Co-Packaged Optics, a packaging technology that integrates optical and electronic components within the same package |
| "DC" | direct current |
| "die" | one single chip cut from a wafer before being packaged |
| "DSmSiP" | Double Side Molded System-in-Package |
| "DS Partial Mold" | Double Side Partial Mold, which protects specific areas using selective molding technology |
| "edge AI" | use of artificial intelligence directly on local devices without utilizing cloud |
| "EMI" | electromagnetic interference |
| "eWLB" | embedded wafer level Ball Grid Array |
| "fabless" | a semiconductor design company that does not own a wafer manufacturing plant and only focuses on design |
| "Fan-In" | packaging method where all electrical connections are confined within the footprint of the chip |
| "Fan-Out" | packaging method with connections fanned-out of the chip surface to enable more external electrical connections |
| "FC" | packaging method where the chip is mounted face-down onto the substrate |

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| "FOCT-S" | Fan-Out Connected Tech-Silicon |
| "FOCT-L" | Fan-Out Connected Tech-Local Silicon Interconnect |
| "frequency" | the rate at which a power electronic device operates. |
| "foundry" | a manufacturer specializing in the production and manufacture of chips in the field of integrated circuits |
| "GaN" | gallium nitride |
| "GPU" | graphic processing unit |
| "HBM" | high bandwidth memory |
| "HPC" | high-performance computing |
| "I/O" | input to receive data and output to send data |
| "IATF16949" | international technical specification of automotive industry quality management system, which prepared by International Automotive Task Force and ISO |
| "IDM" | integrated device manufacturer, a company that takes charge of semiconductor design, manufacturing, packaging and testing |
| "integrated circuit" or "IC" | a structure with specific circuit functions, formed by integrating numerous transistors, resistors, capacitors, and their interconnecting wiring onto a semiconductor chip through a series of semiconductor manufacturing processes |
| "interposer" | a special carrier used to connect multiple chips and other components, which is placed between the bare die and the traditional packaging substrate, achieving precise chip-to-chip connections through redistributed layers |
| "IPD" | Integrated Passive Device, being miniaturized resistors, capacitors, and inductors embedded into a single substrate |
| "ISO" | International Organization for Standard |
| "ISO 14001" | the Environmental Management System published by the ISO |
| "ISO 45001" | the Occupational Health and Safety Management System published by the ISO |
| "ISO 50001" | the Energy Management System published by the ISO |
| "ISO 9001" | the International Quality Management System published by the ISO |

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| "IoT" | the Internet of things |
| "LDFO" | Low-Density Fan-Out |
| "LGA" | Land grid array |
| "LPDDR" | Low-Power Double Data Rate, a type of volatile memory optimized for mobile and embedded devices |
| "LVM" | Low-Volume Manufacturing, a production process designed for small batch sizes rather than mass production |
| "modules" | packaged components that include integrated circuits or other electronic components to build larger systems or devices |
| "Moore era" | the period when semiconductor progress under the Moore's Law that transistor density doubles approximately every two years |
| "OLGA" | Optical Land Grid Array |
| "OSAT" | outsourced semiconductor assembly and test |
| "packaging" | the process of transforming bare semiconductor die (integrated circuit) into a final packaged chip product through a series of technological procedures, while providing physical protection, electrical connection and thermal management |
| "PCB" | printed circuit board |
| "PCT" | Patent Cooperation Treaty |
| "Pi" | polyimide |
| "Post Bump-CP" | post-Bumping chip probing, a testing process performed after the Bumping stage |
| "Pre Bump-CP" | pre-Bumping chip probing, a testing process performed before the Bumping stage |
| "PVD" | physical vapor deposition |
| "QFN" | Quad Flat No-Lead |
| "R&D" | research and development |
| "RDL" | redistribution layers |
| "RF" | radio frequency |

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| "SiP" | System-in-Package |
| "SoC" | System on chip |
| "SOT" | small outline transistor, a compact, surface-mount package used for transistors and other small semiconductors |
| "sq.m." | square meter(s) |
| "substrate" | the base material that provides mechanical support and electrical connections between the chip and the printed circuit board |
| "testing" | the process of detecting the electrical performance, functional integrity, reliability, and environmental adaptability of semiconductors using professional testing equipment, so as to screen out qualified products and eliminate defective ones |
| "TGV" | Through-Glass Via, a vertical electrical interconnect formed through a glass substrate |
| "TMV" | Through-Mold Via, a vertical interconnect structure formed through the mold compound of a semiconductor package |
| "TSV" | Through-Silicon Via, a vertical electrical connection that passes through a silicon wafer or die |
| "TXV" | Through-X-Interposer Via, a vertical interconnect technology that enables high-density electrical connections through interposer materials like glass or silicon |
| "UBM" | Under Bump Metallization |
| "ultra-high-end packaging and testing" | packaging and testing technologies beyond conventional wire-bond and flip-chip methods, enabling higher input/output density, improved signal integrity and enhanced thermal performance for next-generation applications, including FOCT-R, FOCT-S, FOCT-L, CPO, TMV, and TGV |
| "wafer" | a thin slice of semiconductor material, used in the manufacture of integrated circuits and other microelectronic devices |
| "WB" | wire bonding |
| "Wettable Flank" | a treated terminal edge on surface-mount components that allows visible solder wetting |
| "WLP" | Wafer-Level Packaging |
| "X-Sip" | Extended System-in-Package |