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GLOBAL AND CHINA SEMICONDUCTOR MARKET OVERVIEW

Definition of Semiconductor

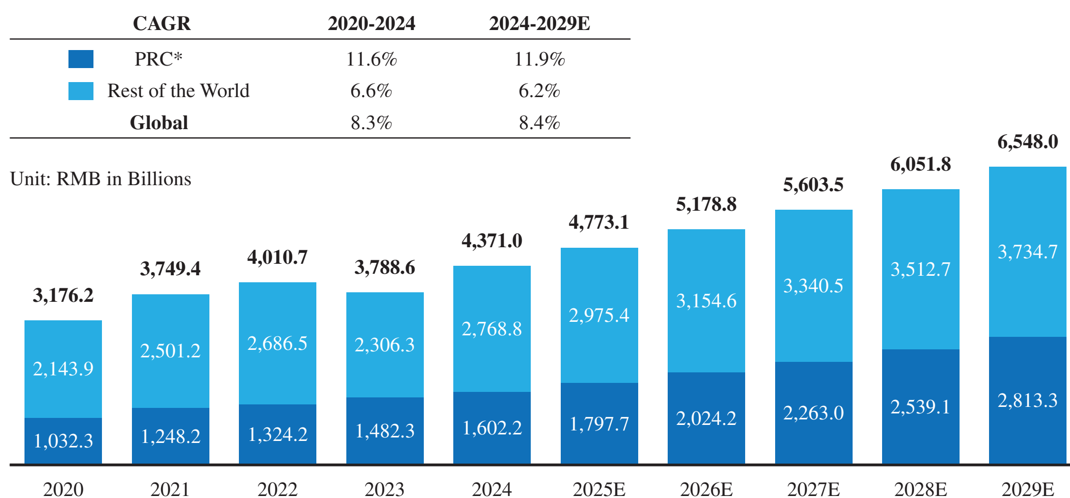
A semiconductor refers to a product that integrates multiple electronic components (such as transistors, resistors, capacitors, etc.) onto a single semiconductor material using miniaturization technology. It boasts advantages including small size, low power consumption, high reliability, and low cost, serving as the core foundation of modern electronic information technology.

Global and China Semiconductor Market Size Analysis

The semiconductor market boasts immense scale and broad prospects. As the global economy evolves and technological innovation advances, semiconductors — recognized as the core of the information technology and electronics industries — are growing increasingly vital. The rapid development of emerging technologies such as AI, 5G, the Internet of Things (IoT), and automotive electronics has spurred robust demand for high-performance, low-power consumption chips, driving sustained growth in the semiconductor market.

The following chart sets forth the actual and estimated market size of the global and China semiconductor market, for the years indicated.

Global and China Semiconductor Market Size



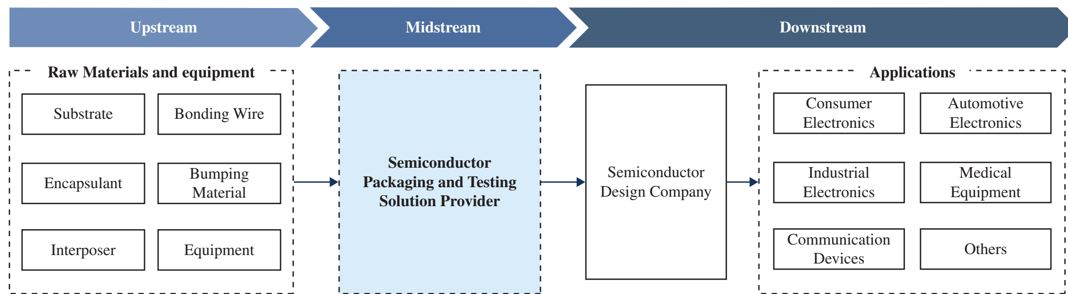
* PRC refers to Chinese Mainland

Source: WSTS, SIA, Frost & Sullivan

GLOBAL AND CHINA SEMICONDUCTOR PACKAGING AND TESTING MARKET

Introduction to Semiconductor Packaging & Testing Industry Chain

The semiconductor packaging and testing industry chain consists of several key segments. In the upstream, raw materials including substrates, bonding wires, encapsulants, bumping materials, interposer, and equipment serve as the foundational input. The midstream features semiconductor packaging and testing solution providers that leverage these upstream raw materials to offer specialized packaging and testing services. This requires them to possess profound expertise in complex packaging technologies, precision testing methodologies, and material science. These packaged and tested products then supply semiconductor design companies. The downstream encompasses a wide range of applications, such as consumer electronics, automotive electronics, industrial electronics, medical equipment, communication devices, and other fields.

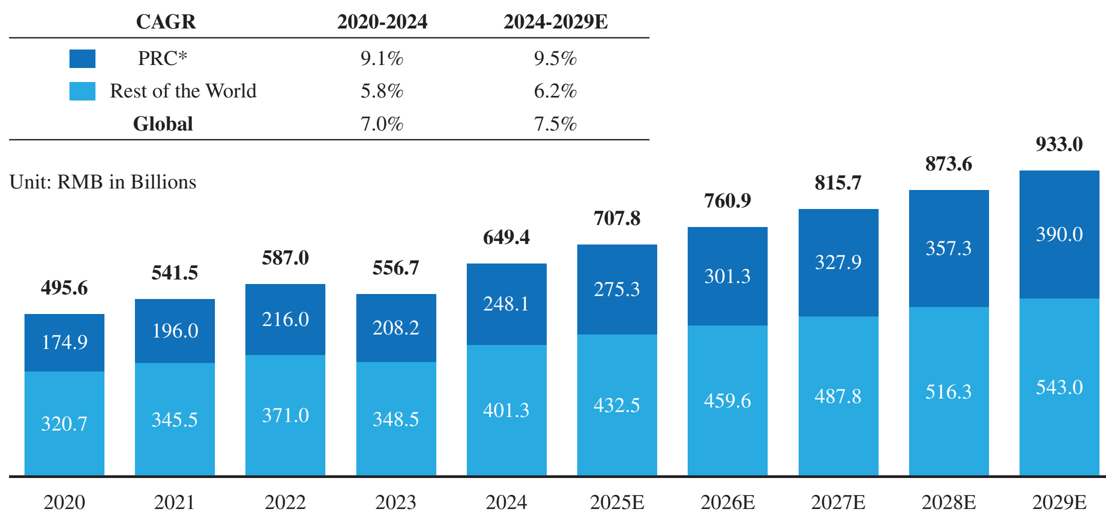


Source: Desk research, Frost & Sullivan

Global and China Semiconductor Packaging & Testing Market Size

Semiconductor packaging involves a series of processes that encapsulate manufactured bare dies or wafers into protective casings, providing physical protection, electrical interconnection, and thermal management so the semiconductors can function as independent devices in a wide range of electronic equipment; semiconductor testing uses specialized equipment to evaluate electrical performance, functional integrity, reliability, and environmental adaptability, enabling the screening of qualified products and the removal of defective ones. The global semiconductor market boasts enormous potential and vast space. Spurred by the vigorous development of fields like consumer electronics, automotive electronics, and industrial control, which boosted the demand for semiconductors. The following chart presents the actual and estimated market size of the global and China semiconductor packaging & testing market, for the years indicated.

Global and China Semiconductor Packaging & Testing Market Size



* PRC refers to Chinese Mainland

Source: WSTS, SIA, Frost Sullivan

Market Drivers and Trends of Semiconductor Packaging and Testing Industry

- ***The Growth of Semiconductors Drives the Expansion of the Packaging & Testing Industry***

The demand for semiconductors has surged across multiple fields such as consumer electronics and automotive electronics. Technologies like 5G and AI have spurred the demand for high-performance chips, fueling the expansion of the semiconductor market. This provides a steady stream of orders for the packaging and testing industry, whose market scale has grown steadily in tandem with the semiconductor sector and is expected to maintain a high growth rate in the future.

- ***Bottlenecks in Process Miniaturization Drive the Development of Advanced Packaging***

As chip process nodes shrink to 7nm, 5nm, and beyond, they face physical and cost challenges — making advanced packaging a key breakthrough. Advanced packaging technologies enhance chip performance and integration while reducing costs through innovative interconnection and integration solutions, thereby driving technological innovation and value enhancement in the packaging and testing industry.

- ***OSATs Strengthen Collaboration with Upstream and Downstream Sectors***

With the refinement of industrial division of labor, OSATs (Outsourced Semiconductor Assembly and Testing companies) have deepened collaboration with upstream and downstream partners. They jointly optimize designs with Fabless companies to provide customized solutions for downstream clients, and work with Foundries to ensure smooth workflow. These efforts collectively promote the development of packaging industry, improve packaging efficiency and quality, and enhance the overall competitiveness of the industrial chain.

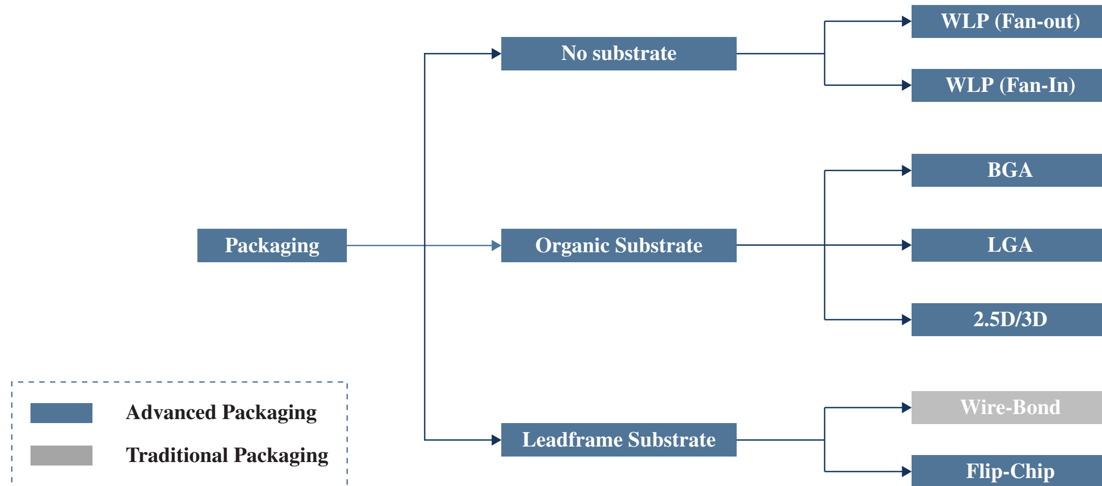
OVERVIEW OF GLOBAL ADVANCED PACKAGING & TESTING MARKET

Definition of Advanced Packaging

Advanced packaging refers to a packaging solution with process complexity, achieved through the application of innovative structural design, interconnection technology, materials, and equipment. It helps realize higher integration, better performance, smaller size, lower power consumption, and higher reliability of semiconductor. It is not only a key post-process in semiconductor manufacturing but also a core technical path to continue the improvement of semiconductor performance and meet the complex application demands of downstream industries against the background of the slowing down of Moore's Law.

Classification of Semiconductor Advanced Packaging

Due to the differences in electrical performance, size, application scenarios and other factors of different semiconductor products, the packaging forms are diverse and complex. According to whether there are a packaging substrate and the material of the packaging substrate, semiconductor packaging products can be divided into different categories. Among them, there are different packaging technologies in each category. The following presents the classification of typical packaging technologies.



Source: Guidance Catalog for Industrial Structure Adjustment (2024 Edition), Frost & Sullivan

The Group's Advanced Packaging portfolio comprises BGA, LGA, WLP, 2.5D/3D, as well as FC-QFN and FC-SOT, while its Traditional Packaging offerings include WB-QFN.

Traditional packaging primarily provides chip protection, size enlargement, and electrical connection by linking the die to external circuits through methods such as wire bonding, while also offering mechanical protection and heat dissipation; advanced packaging builds on these core functions by further improving functional density, shortening interconnection lengths, and enabling system-level reconstruction, thereby increasing product integration and functional diversification without relying on breakthroughs in chip manufacturing processes.

Comparison Between Advanced Packaging and Traditional Packaging

Packaging Type	Traditional Packaging	Advanced Packaging	
Technology Type	Leadframe wire-bond	BGA	2.5D/3D
System Memory Bandwidth	Low	Medium	High
Chip Power Ratio	Low	Medium	High
Chip Size	Large	Small	Small
Heat Dissipation Efficiency	Low	High	High
Packaging Cost	Low	Medium	High
Performance	Low	Medium	High
Packaging Form	With lead frames as the carrier, chip and external pins are connected unidirectionally through wire bonding. The package size is much larger than the chip, and the number of pins is small and distributed sparsely.	By means of Redistribution Layer (RDL), interposer or vertical stacking structure, technologies such as flip-chip bonding and Through-Silicon Via (TSV) are adopted to realize high-density interconnection of multiple chips. The package size is close to the chip, and the integration degree and performance are greatly improved.	

Packaging Type	Traditional Packaging	Advanced Packaging
Global Demand Growth Rate	2020-2024: 4.6% 2025E-2030E: 3.9%	2020-2024: 9.9% 2025E-2030E: 10.9%

Source: WSTS, Public Information, Frost & Sullivan

Global and China Semiconductor Advanced Packaging & Testing Market Size

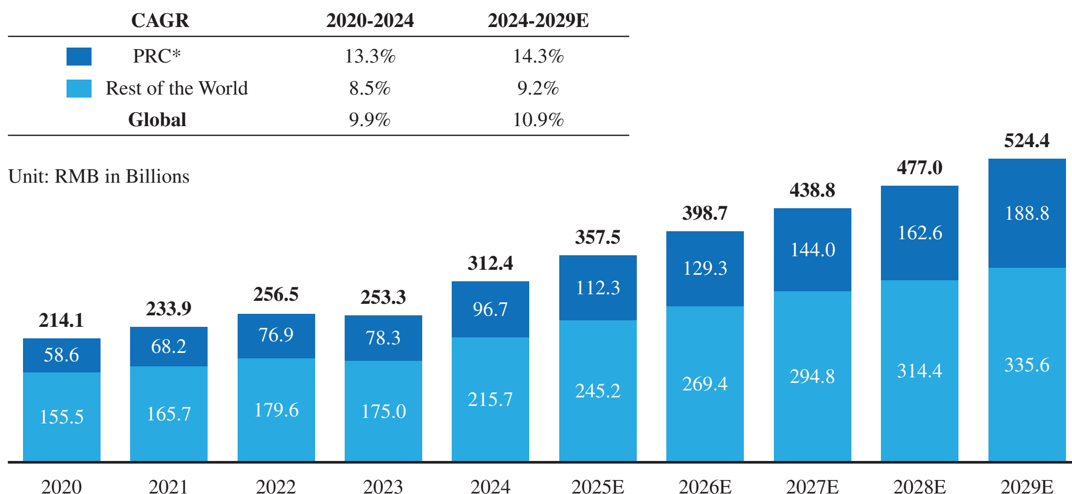
Driven by the demand for high-integration and low-power consumption chips in the fields of communications, consumer electronics, high-performance computing, and artificial intelligence, the market scale of the advanced semiconductor packaging and testing industry — backed by technologies such as flip-chip bonding, wafer-level packaging, and 2.5D/3D packaging — has achieved rapid growth, emerging as one of the segments with leading growth rates in the semiconductor industry chain.

Over the next five years, as Moore's Law slows down, advanced packaging and testing — serving as a core path to enhance chip performance — will further benefit from the popularization of autonomous driving, data centers, high-performance computers, and smart wearable devices, as well as the maturity of cutting-edge packaging and testing technologies. It will maintain a robust growth momentum, with its market scale expected to expand steadily. In contrast to traditional packaging, which features relatively low added value and a saturated market, advanced packaging boasts high technical barriers and supply scarcity. Its unit price and demand growth rate are significantly higher, enabling its market scale to outperform the overall packaging and testing industry in terms of growth rate over the long term.

The PRC market has delivered outstanding performance. Although the PRC still lags behind some overseas markets in advanced packaging and testing technologies, Chinese enterprises have made aggressive investments in advanced packaging and testing technologies and production capacity scale to meet the rapidly growing downstream demand.

The following chart sets forth the actual and estimated market size of the global and China semiconductor advanced packaging & testing market, for the years indicated.

Global and China Semiconductor Advanced Packaging & Testing Market Size



* PRC refers to Chinese Mainland

Source: WSTS, SIA, Frost & Sullivan

Market Drivers and Trends of Semiconductor Advanced Packaging and Testing Industry

Multi-sector demand fuels advanced packaging and testing market. The semiconductor advanced packaging and testing market is largely driven by its diverse applications across sectors like high-performance memory, data centers, automotive, and consumer electronics. Technologies like 3D NAND and HBM address AI and data volume demands, while data centers leverage Chiplet heterogeneous integration for better computing power and energy efficiency. Automotive and consumer electronics require compact, reliable, and efficient solutions, further fueling the adoption of advanced packaging.

Rising status of the packaging segment in the industrial chain. As semiconductor process technologies hit physical limits, advanced packaging's role in system-level integration and performance enhancement has become increasingly vital. It is no longer just about chip protection or connection, but a key strategy for companies to boost competitiveness and meet emerging semiconductor needs.

Advanced packaging technologies moving toward high performance and miniaturization. The demand for smaller and higher-performing devices has pushed advanced packaging toward miniaturization and enhanced performance. 2.5D/3D packaging and wafer-level packaging (WLP) are critical for supporting AI, data centers, and consumer electronics with improved integration, speed, and reduced size, overcoming technical bottlenecks.

Accelerating localization in advanced packaging and testing. The localization trend in advanced packaging and testing is accelerating, driven by changing trade environments and the push for independent semiconductor development, particularly in China. Domestic manufacturers are making strides in localized production, and as R&D and investment grow, this trend is expected to intensify, further reducing dependence on foreign technologies.

COMPETITIVE LANDSCAPE OF SEMICONDUCTOR ADVANCED PACKAGING AND TESTING MARKET

Ranking of Semiconductor Advanced Packaging and Testing

There are a large number of participants in PRC's semiconductor packaging and testing market, with approximately 150 to 200 OSATs. Most of these OSATs are mainly engaged in traditional packaging and testing businesses. They generally have small overall revenue scales, and the proportion of revenue from advanced packaging and testing in their total revenue is relatively low.

In addition, affected by the wide variety of semiconductor products, two types of OSATs have been formed in the market, which are General-Purpose OSATs and Application-Specific OSATs. General-Purpose OSATs offer packaging and testing services for many different types of chips used in various fields. They do not focus on just one chip type; instead, they have flexible capabilities to serve a wide range of customer needs. Application-Specific OSATs specialize in packaging and testing only chips for specific uses. Their technologies and processes are tailored to meet the unique requirements of these niche fields, rather than serving all chip types and industries. In terms of the total revenue of semiconductor packaging and testing, our company ranked 7th in PRC's General-Purpose OSAT companies.

In terms of the revenue in 2024, our Company ranked 7th among general-purpose semiconductor OSAT in PRC, with a market share of 0.6%.

Ranking of China's General-Purpose OSAT Companies, by Revenue of Semiconductor Advanced Packaging and Testing in 2024

Ranking	Company	Revenue in Billion RMB	Market Share	Listed Status
1.	Company A	25.8	26.7%	Listed
2.	Company B	16.0	16.6%	Listed
3.	Company C	9.7	10.0%	Listed
4.	Company D	5.6	5.8%	Unlisted
5.	Company E	4.7	4.9%	Listed
6.	Company F	2.3	2.3%	Listed
7.	The Company	0.6	0.6%	Unlisted
8.	Company G	0.3	0.3%	Listed

Source: Annual Report, Expert Interview, Frost & Sullivan

Notes:

(1) Company A is a public company founded in 1972 and is listed on Shanghai Stock Exchange. It provides semiconductor chip manufacturing services with a focus on packaging, assembly and test solutions for automotive, high-performance computing, memory and consumer applications.

(2) Company B is a public company founded in 1997 and is listed on Shenzhen Stock Exchange. It is an OSAT company that focuses on advanced packaging solutions for high-performance computing, automotive, memory and other applications.

(3) Company C is a public company founded in 2003 and is listed on Shenzhen Stock Exchange. It provides packaging and testing services for consumer, industrial, and automotive semiconductor products.

(4) Company D is a private company founded in 2017 and is headquartered in Beijing. It provides packaging and testing services across discrete, analog, RF and other chip segments.

(5) Company E is a public company founded in 2014 and is listed on Shanghai Stock Exchange. It specializes in wafer-level advanced packaging, multi-die chiplet integration, and related services for semiconductor products.

(6) Company F is a public company founded in 2017 and is listed on Shanghai Stock Exchange. It provides packaging and test services with emphasis on advanced packaging technologies.

(7) Company G is a public company founded in 2006 and is listed on Shanghai Stock Exchange. It is an advanced-packaging service provider.

The following chart illustrates the range of packaging technologies adopted by leading OSAT companies based on publicly available information. The company possesses core mass production capabilities in 2.5D, bumping, Fan-out WLP, Fan-in WLP, WB/FC-BGA, WB/FC/Hybrid/SiP-LGA, and FC-QFN technologies. In addition, it is actively promoting the R&D and industrialization of cutting-edge technologies such as Chiplet interconnection (homogeneous and heterogeneous chip integration), optoelectronic sensing, and TGV glass substrate products. The company is among the few domestic advanced packaging service providers that have achieved comprehensive capabilities across all of the above technologies.

Packaging Technology		The Company	Company A	Company B	Company C	Company D	Company E	Company F	Company G
2.5D/3D	FOCT-R/S/L	√	√	√	√	×	√	√	×
	TGV	√	√	√	√	×	√	×	×
WLP	Fan-out WLP	√	√	√	√	√	√	√	×
	Fan-in-WLP	√	√	√	√	√	√	√	×
	BUMPING	√	√	√	√	√	√	√	×
BGA	WB/FC-BGA	√	√	√	√	√	√	√	√
	Hybrid-BGA	√	√	√	√	√	×	√	×
LGA	WB/FC-LGA	√	√	√	√	√	×	√	√
	Hybrid-LGA	√	√	√	√	√	×	√	√
FC-QFN		√	√	√	√	√	×	√	√

Source: Public Information, Frost & Sullivan

Note:

(1) "√" indicates disclosed coverage, while "×" indicates undisclosed coverage.

Entry Barriers of Semiconductor Advanced Packaging Industry

- ***High-Barrier Technological R&D and Process Accumulation***

Advanced packaging relies on precision technologies such as microbump bonding, hybrid bonding, and TSV (Through-Silicon Via). It requires long-term investment to overcome challenges in material compatibility and thermal management. Enterprises must possess interdisciplinary R&D capabilities, while process stability needs to be verified through massive volume production — making it difficult for new entrants to break through technical barriers in the short term.

- ***Reserve of High-End Talents and Cross-Domain Experience***

Advanced packaging demands collaboration among talents in multiple fields, including packaging engineering, materials science, and chip design. Senior technical teams need to master cutting-edge processes and failure analysis capabilities. New enterprises struggle to quickly build core teams, and the experience gap restricts technology implementation and mass production stability.

- ***Heavy Asset Investment and Capacity Scale Thresholds***

OSATs (Outsourced Semiconductor Assembly and Testing companies) need huge capital to construct high-cleanliness production lines and purchase advanced packaging equipment and testing systems, with a single factory investment often reaching billions of yuan. Meanwhile, they must achieve economies of scale to dilute costs. Small and medium-sized players, due to insufficient funds, find it hard to bear equipment depreciation and continuous capacity expansion pressure.

- ***In-Depth Linked Industrial Chain Collaboration Capabilities***

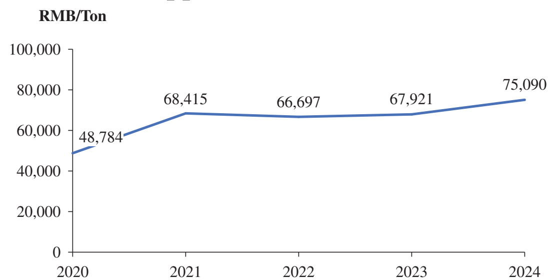
OSATs need to collaborate deeply with Fabless companies and Foundries, and participate in the optimization of packaging solutions during the chip design phase. Leading enterprises have accumulated customer trust through long-term cooperation, while new entrants face difficulties in quickly establishing stable supply chains and customer relationships — making it challenging to secure high-end orders.

COST ANALYSIS

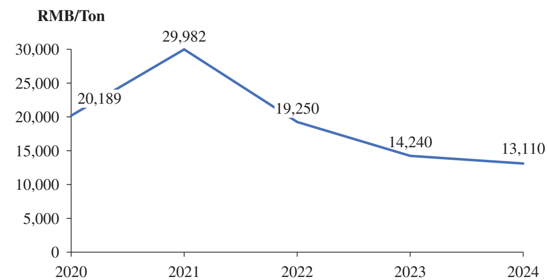
Semiconductor packaging and testing is a materials-driven manufacturing business. Materials typically account for more than 50% of cost of sales, while the remainder mainly consists of manufacturing expenses such as labor, depreciation and factory overhead, plus testing costs. In substrate-based advanced packages such as FC-BGA, the IC substrate is often the largest single cost item and can reach about 50% of total packaging cost. Electrolytic copper and epoxy resin are heavily used within the IC substrate: copper primarily appears as electrolytic copper foil and plated copper features that form the substrate wiring and interconnect structures, while epoxy-resin systems are widely used in dielectric build-up films such as ABF and in resin systems within laminate materials. As a practical rule of thumb for ABF substrates, copper-linked inputs typically represent around 10% -20% of substrate cost, and epoxy-resin-linked inputs typically represent around 25% -35% of substrate cost, so changes in these two prices can meaningfully affect the substrate portion of total packaging cost.

From 2020 to 2024, the cost structures in China's semiconductor packaging and testing industry exhibited a significant divergence. Electrolytic copper prices experienced a volatile uptrend, peaking at an average of 75,090 RMB/ton in 2024, while epoxy resin followed a "peak-and-plunge" trajectory, retreating to a five-year low of 13,110 RMB/ton. Regarding supply, the copper market remains tight due to global mining disruptions and surging demand from the EV and AI sectors; conversely, the epoxy resin market has shifted toward oversupply following aggressive domestic capacity expansions. For companies focused on advanced solutions, the impact of surging metal costs is relatively mitigated. Instead, the persistent deflation in resin costs significantly lowers the procurement expenses for molding compounds and substrates, providing a strategic advantage to maintain price competitiveness.

Average Market Price of Electrolytic Copper, China, 2020-2024



Average Market Price of Epoxy Resin, China, 2020-2024



Source: Choice, Oilchem, Frost & Sullivan

SOURCES OF INFORMATION AND RESEARCH METHODOLOGY

We engaged Frost & Sullivan for preparing an independent industry report in respect of the [**REDACTED**]. The information from Frost & Sullivan disclosed in the document is extracted from the Frost & Sullivan Report, a report commissioned by us for a fee of RMB400,000, and is disclosed with the consent of Frost & Sullivan. The Frost & Sullivan Report has been prepared by Frost & Sullivan independently without any influence from us or other interested parties. Frost & Sullivan is an independent global consulting firm founded in 1961 in New York, Its services include, among others, industry consulting, market strategic consulting and corporate training. Frost & Sullivan conducted (i) primary research, which involved discussing the status of the industry with certain leading industry participants, and interviews with industry experts on a best-effort basis to collect information in aiding in-depth analysis; and (ii) secondary research, which involved reviewing government statistics, industry association publication, company reports, independent research reports and data based on its own research database. Our Directors confirm that, to the best of their knowledge, after making reasonable inquiries, there is no material and adverse change in the market information since the date of the Frost & Sullivan Report which may qualify, contradict or have an impact on the information in this section.