GLOSSARY OF TECHNICAL TERMS

"AI"	artificial intelligence
"AMOLED"	active-matrix organic light-emitting diode
"AOI"	automated optical inspection
"ATE	automatic test equipment
"Bumping"	a front-end advanced packaging process in which metal bumps are formed on the pads of a wafer through processes such as sputtering, lithography, electrochemical deposition and wet etching; replaces traditional wire bonding and enables high-density interconnections, higher I/O counts and improved electrical performance
"Bumps"	microscopic interconnect structures formed on the bond pads of a wafer during the bumping process, enabling point-to-point electrical signal transmission and replacing traditional wire bonding in advanced packaging applications
"CAGR"	compound annual growth rate
"COF"	chip-on-film
"COG"	chip-on-glass
"CP"	chip probing
"CPK"	Complex Process Capability index
"DDIC"	display driver integrated circuit
"DRAM"	dynamic random-access memory
"Electrochemical Deposition"	a manufacturing process that uses electrical current to coat a solid substrate with a thin, adherent layer of metal or a metallic compound
"Electroplating"	a process step in bumping in which the wafer is immersed in an electroplating solution and, when an external current is applied, metal ions are reduced and deposited selectively within photoresist openings to form bumps
"Etching"	a precision manufacturing step in the bumping process used to remove excess gold and titanium-tungsten layers between bump sites after photoresist removal, completing the fabrication of individual bumps
"Fabless"	a business model in which a company designs integrated circuits but outsources fabrication (and often packaging and testing) to third-party manufacturers; contrasted with the IDM model
"Flip chip"	an advanced semiconductor packaging technology where the silicon die is flipped upside down and directly connected to the substrate
"HBM"	high bandwidth memory

GLOSSARY OF TECHNICAL TERMS

"Heterogeneous Integration"	an advanced packaging approach that integrates multiple chips or chiplets of different functionalities, materials or process nodes into a single package to achieve higher system performance
"HITS"	high-speed interconnect technology solutions
"IC"	integrated circuit
"IDM"	integrated Device Manufacturer
"I/O"	input/output
"Interposer"	a semiconductor substrate placed between chips to enable high-density interconnection in advanced multi-chip packaging; used to integrate logic chips and high-bandwidth memory
"IP"	intellectual property
"LCD"	liquid crystal display
"Lithography"	a precision process step in bumping in which a photoresist layer is applied to the wafer, exposed through a photomask to define the bump pattern, and then developed to open windows for subsequent bump formation
"LPDDR"	Low Power Double Data Rate, a low-power memory technology for smartphones, tablets and thin laptops
"Memory IC"	a type of integrated circuit used to store data
"Mini-LED"	an advanced display backlighting technology using very small LED chips; referenced as an emerging display technology penetrating high-end vehicle models alongside AMOLED
"OLED"	organic light-emitting diode
"OSAT"	outsourced semiconductor assembly and testing
"Photomask"	a plate used in lithography to define the bump pattern on a wafer during the exposure step
"Photoresist"	a light-sensitive material applied to a wafer surface during lithography to define areas for bump formation; removed after electroplating as part of the etching process
"Polyimide"	a high-performance polymer used as the base film material in COF substrates, providing flexibility, thermal stability and electrical insulation
"Probe Card"	a precision interface component used in chip probing that makes electrical contact with individual dies on a wafer to test their electrical characteristics
"R&D"	research and development
"RDL"	redistribution layer

GLOSSARY OF TECHNICAL TERMS

"SoC"	system-on-chip
"Sputtering"	a physical vapor deposition process used in bumping in which high-energy ions bombard metal targets (typically titanium-tungsten and gold) causing atoms to be ejected and deposited onto the wafer surface to form the UBM layer
"TSV"	through-silicon via
"UBM"	under-bump metallization
"Wafer Dicing"	the process of cutting a processed semiconductor wafer into individual dies (chips); a step following bumping and chip probing in the packaging flow, at which defective dies (marked by ink) are removed
"Wafer Grinding"	a critical semiconductor manufacturing process that reduces the thickness of silicon wafers to allow for smaller, stacked, and high-performance microchips
"Wire Bonding"	a traditional packaging interconnect method using thin metal wires to connect a die to a substrate or lead frame; partially replaced by bumping technology in advanced packaging applications due to bumping's higher I/O density and performance advantages