Certain information and statistics set out in this section have been extracted from various official government publications, market data providers and a report commissioned by the Company and prepared by an independent third party, Frost & Sullivan. The information from official government sources has not been independently verified by the Company, the Sole Sponsor, the Sole Sponsor-Overall Coordinator, the Sole Overall Coordinator, [REDACTED] or any of their respective directors, officers, employees, agents, advisers or representatives or any other parties involved in the [REDACTED], and no representation is given as to its accuracy, fairness and completeness.

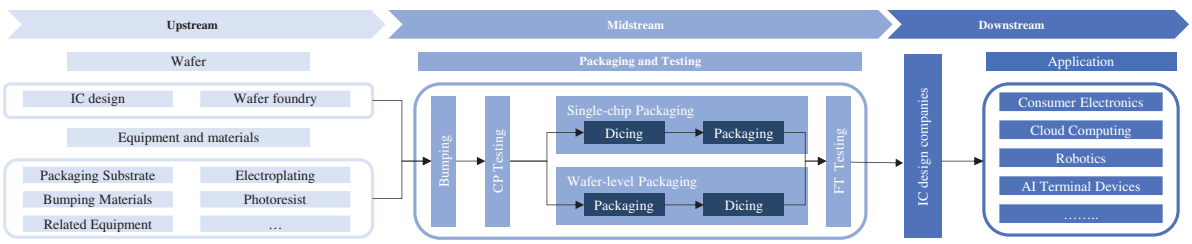
OVERVIEW OF THE GLOBAL SEMICONDUCTOR ADVANCED PACKAGING AND TESTING INDUSTRY

Definition and Classification of Semiconductor Packaging and Testing

The semiconductor packaging and testing industry occupies a critical position in the latter stage of the semiconductor industry chain, serving as a vital bridge between wafer fabrication and end-use applications. After completing wafer manufacturing, chips remain in bare die form and must undergo packaging to form devices with physical protection, electrical connectivity, and thermal management capabilities, followed by testing to verify performance and reliability before entering downstream applications.

Packaging refers to the process of forming independent electronic devices with structural stability and environmental adaptability from semiconductor bare dies through welding, interconnection, and packaging materials. Beyond providing physical protection, packaging enables signal transmission and thermal management through internal interconnect structures, serving as a critical safeguard for reliable chip operation. Testing, on the other hand, spans both the wafer stage and the finished product stage. As chip complexity continues to increase, packaging and testing has evolved from a mere "post-manufacturing process" into a significant factor influencing chip performance.

Value Chain of Packaging and Testing in IC Industry



The upstream primarily includes packaging material and equipment suppliers, covering integrated circuit (IC) substrates, packaging adhesives, bonding wires, bump materials, and related production equipment. The performance of raw materials and the precision of equipment directly affect packaging yield and product reliability, and serves as the basis for packaging and testing companies to achieve stable mass production. In the advanced packaging sector, the importance of high-density interconnect materials and high-precision equipment increases further, imposing more stringent requirements on material performance and manufacturing precision.

The midstream comprises packaging and testing service providers, including outsourced semiconductor assembly and test (OSAT) companies as well as internal packaging and testing divisions of certain integrated device manufacturers (IDMs). Through packaging design, manufacturing, and testing verification, these companies transform wafers into ready-to-use semiconductor devices. During the traditional packaging phase, the midstream's core competitive advantage lies in large-scale manufacturing capability. In the advanced packaging phase, companies are required to possess high-density interconnect, multi-chip integration, and system-level testing capabilities, with substantially higher technical barriers and capital requirements.

The downstream primarily includes fabless design companies, IDMs, and end-system manufacturers, with applications spanning consumer electronics, cloud computing, robotics, and artificial intelligence (AI) terminal devices. The increasing intelligence of terminal products drives growth in chip usage and performance requirements, fueling demand for high-value-added packaging solutions.

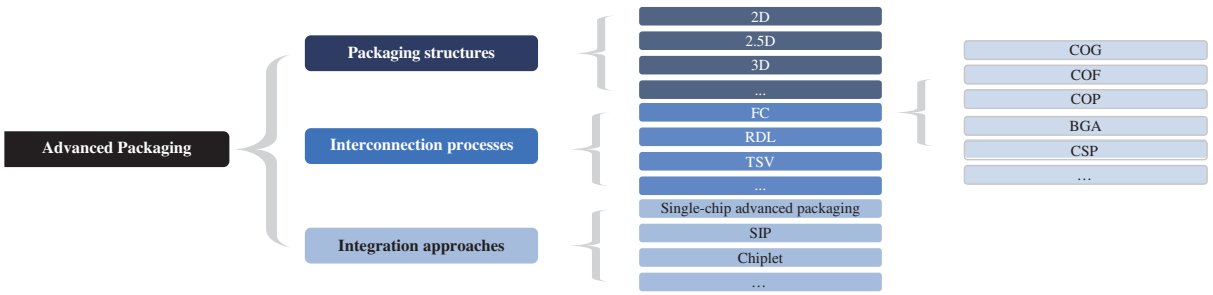
Definition of Semiconductor Advanced Packaging

Advanced packaging refers to packaging technologies that, in the context of slowing semiconductor process node scaling, significantly enhance chip functional density, interconnect density, electrical performance, or thermal performance through structural innovation and process upgrades at the packaging level, without further reducing wafer manufacturing nodes. Compared with traditional packaging, advanced packaging demonstrates significant innovation in structural form, interconnect processes, or integration methods, and serves as a key technological pathway for continued advancement in semiconductor performance.

Classified by interconnect processes, advanced packaging primarily involves high-density interconnect technologies such as flip chip interconnect (FC), wafer-level redistribution layer (RDL), and through-silicon via (TSV) vertical interconnect. ~Among these, Flip chip serves as one of the most widely adopted and foundational interconnect technologies in advanced packaging by forming bumps on chip pads and directly bonding chips to substrates, thereby improving I/O density, transmission efficiency and electrical performance. Building on FC technology, packaging forms such as chip-on-glass (COG), chip-on-film (COF) and chip-on-plastic (COP) are widely used in display driver IC (DDIC) applications to support lightweight, high-density and flexible display integration. In addition, ball grid array (BGA) and chip scale package (CSP) technologies are broadly adopted in memory, processor and consumer electronic applications due to their advantages in package size, electrical performance and heat dissipation capability. Wafer-level redistribution layer interconnect forms metal redistribution layers on chip surfaces to optimize pad layouts and support high-density wiring, serving as a core process for wafer-level packaging technologies. Through-silicon via vertical interconnect establishes vertical electrical channels through silicon wafers, enabling higher integration density and supporting heterogeneous integration and chip stacking architectures.

Classified by structural form, advanced packaging can be divided into 2D packaging, 2.5D packaging, and 3D packaging. 2D packaging achieves chip-to-substrate interconnection within the substrate plane. 2.5D packaging introduces silicon interposers or high-density redistribution boards between the chip and substrate, enabling higher-density cross-chip interconnections through redistribution layers (RDL) and micro-bumps. Representative technologies include Chip on Wafer on Substrate (CoWoS) and Embedded Multi-Die Interconnect Bridge (EMIB). 3D packaging achieves chip stacking interconnections in the vertical dimension using through-silicon via (TSV) technology, further enhancing functional density and transmission efficiency.

Classified by integration methods, advanced packaging can be divided into single-chip advanced packaging, system-in-package (SIP), and chiplet packaging. Single-chip advanced packaging upgrades the packaging process for a single chip and represents an important component of the current advanced packaging market. System-in-package integrates chips with multiple functions into the same package to achieve system-level functionality. Chiplet packaging splits a single system-on-chip (SoC) into multiple independent functional chiplets, which are manufactured separately and then integrated through high-density interconnections.



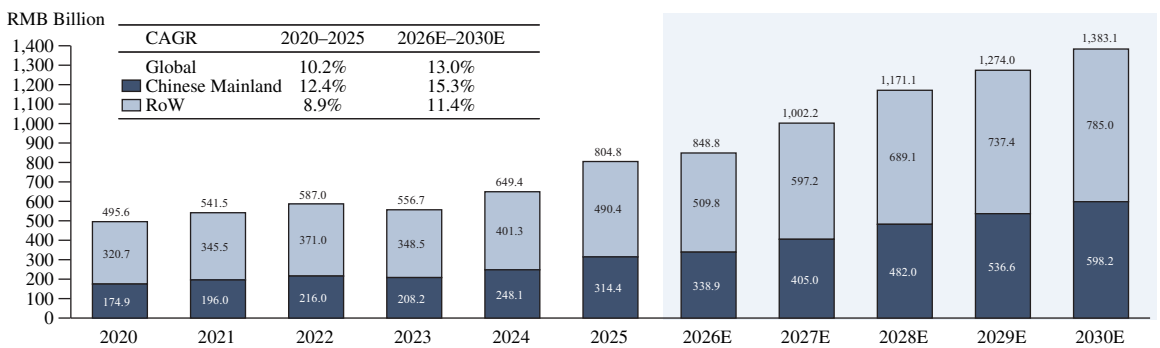
Source: Frost & Sullivan

Market Size of Global Semiconductor Advanced Packaging and Testing

With demand recovery in consumer electronics, automotive electronics, and industrial control sectors, semiconductor shipments have increased, thereby driving synchronous expansion in packaging and testing demand. The global semiconductor packaging and testing market expanded from RMB495.6 billion in 2020 to RMB804.8 billion in 2025, representing a compound annual growth rate (CAGR) of 10.2% from 2020 to 2025. As application scenarios including artificial intelligence (AI), large model training, data center construction, and edge computing continue to expand, high-performance chip demand is expected to further drive overall packaging and testing market growth. The market is projected to grow at a CAGR of 13.0% from 2026 to 2030, reaching RMB1,383.1 billion by 2030.

As a major global electronics manufacturing and end-use application market, Chinese packaging and testing companies have captured a significant share of mid-to-high-end packaging capacity, demonstrating strong industrial clustering effects and scale expansion capability. The Chinese semiconductor packaging and testing market expanded from RMB174.9 billion in 2020 to RMB314.4 billion in 2025, representing a CAGR of 12.4% from 2020 to 2025. It is projected to grow at a CAGR of 15.3% from 2026 to 2030, reaching RMB598.2 billion by 2030.

Market Size of Global and Chinese Mainland Semiconductor Packaging and Testing, by Revenue, 2020–2030E



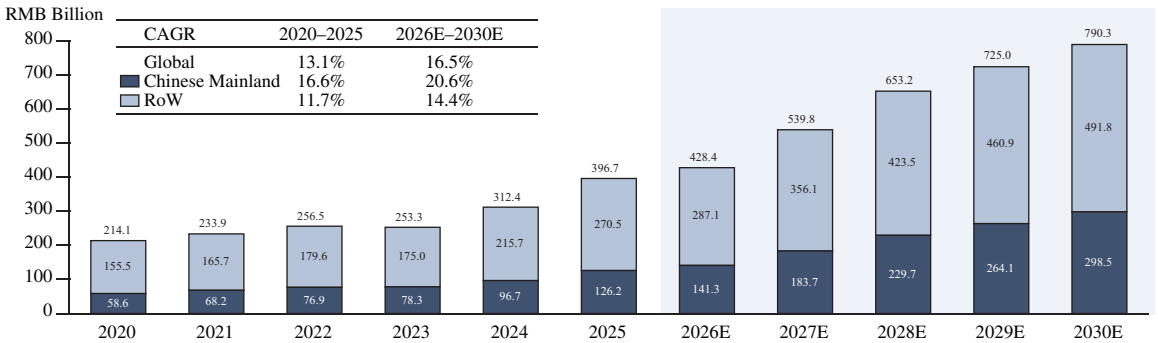
Source: WSTS, SIA, Frost & Sullivan

As downstream applications increasingly demand miniaturization, high performance, low power consumption and high-speed data transmission, advanced packaging has emerged as a key technology pathway for enhancing system performance. Through high-density interconnection, vertical stacking and heterogeneous integration, advanced packaging continuously improves chip integration, bandwidth performance and transmission efficiency, while enhancing system reliability and energy efficiency. Among these technologies, bumping serves as a core foundational process for establishing electrical connections between chips, substrates and other components, forming an important enabling technology underpinning advanced packaging and benefiting from the increasing

adoption of advanced packaging solutions. The global advanced packaging market expanded from RMB214.1 billion in 2020 to RMB396.7 billion in 2025, representing a CAGR of 13.1% from 2020 to 2025. It is projected to grow at a CAGR of 16.5% from 2026 to 2030, reaching RMB790.3 billion by 2030.

Chinese Mainland occupies an important position in the global electronics manufacturing and end-use application market, with rapidly growing downstream application demand driving synchronous expansion in advanced packaging demand. The Chinese mainland advanced packaging market expanded from RMB58.6 billion in 2020 to RMB126.2 billion in 2025, representing a CAGR of 16.6% from 2020 to 2025. It is projected to grow at a CAGR of 20.6% from 2026 to 2030, reaching RMB298.5 billion by 2030.

Market Size of Global and Chinese Mainland Advanced Packaging and Testing, by Revenue, 2020–2030E



Source: WSTS, SIA, Frost & Sullivan

Growth Drivers for the Global Semiconductor Advanced Packaging and Testing Market

Expansion of diverse downstream application demand. As application scenarios such as consumer electronics, new energy vehicles, industrial automation, and data centers continue to expand, semiconductor shipment volumes have grown. The increasing intelligence of terminal products has significantly elevated chip quantity and performance requirements per device. Particularly in new energy vehicles and data centers, demand for high-reliability and high-computing-power chips has grown notably, driving demand for high-value-added packaging solutions.

Rising manufacturing costs driving packaging and testing technology upgrades. As advanced process nodes continue to scale, research and development (R&D) costs and capital expenditures have continuously increased, while wafer manufacturing complexity has significantly risen, with per-unit performance improvement costs continuously escalating. In this context, the marginal benefit of relying solely on front-end scaling to achieve performance improvements has progressively declined. Achieving system-level integration and heterogeneous integration through advanced packaging has emerged as a critical pathway for enhancing computing power and optimizing cost structures.

Rapid growth in advanced packaging and testing demand driven by cloud AI and data infrastructure upgrades. As large model training, inference, and AI-generated content (AIGC) applications continue to deploy to the cloud, cloud service providers are continuously increasing investment in computing power infrastructure, driving rapid growth in demand for high-bandwidth, high-capacity, high-performance memory chips. In addition, FC and BGA packaging technologies are widely adopted in high-performance processors, GPUs and memory-related applications due to their advantages in input/output density, electrical performance and heat dissipation capability, further supporting demand for advanced packaging solutions. High-bandwidth memory (HBM) and high-capacity DRAM products, to meet higher bandwidth, lower latency, and higher energy

efficiency requirements of cloud AI workloads, typically require 2.5D, 3D, and other advanced packaging solutions, thereby driving release of advanced packaging and testing demand for high-end memory chips. Meanwhile, the continuous growth in cloud data volume also drives the expansion and upgrade data center servers, enterprise solid state drives (SSDs), and memory modules, further supporting memory chip packaging and testing demand.

Development Trends in the Global Semiconductor Advanced Packaging and Testing Market

Upgraded computing power demand driving advanced packaging penetration. As the scale of AI training and inference applications continues to expand, demand for high-computing-power chips has grown rapidly. Chip architectures are progressively evolving toward multi-chip integration and heterogeneous integration, with advanced packaging serving as a key technological foundation supporting these architectures. Under this trend, advanced packaging's share of the overall packaging and testing market has continuously increased, with industry growth structure gradually shifting from traditional packaging-driven to advanced packaging-driven. The elevation of technical complexity and added value has also driven packaging and testing companies toward transformation into system-level solution providers.

The post-Moore's Law era reinforcing packaging value. As advanced process costs continue to rise and technical difficulties increase, the pathway of relying solely on transistor scaling to achieve performance improvements has becoming increasingly constrained. Packaging technology plays an increasingly important role in enhancing system performance through improving interconnect density and enabling multi-chip collaboration. The strategic position of the packaging segment in the industry chain has risen, with advanced packaging gradually transitioning from a supporting process to a core performance enhancement method, driving the industry toward high-end and high-technical-barrier development.

Competitive Landscape of the Global and Chinese Mainland Advanced Packaging Industry

Benefiting from the rapid growth of Chinese Mainland's high-end chip design industry and the sustained expansion of wafer manufacturing capacity, demand for advanced packaging has risen in tandem. The three leading companies, leveraging their scale accumulation and long-term cultivation of customer relationships, hold relatively dominant market positions, while other players each demonstrate competitive characteristics rooted in differentiated processes and specialized segments. Our advanced packaging business achieved revenue of RMB1.58 billion in 2025, with a market share of approximately 1.3%, ranking eighth in the industry.

Competitive Landscape of the Chinese Mainland Domestic Advanced Packaging and Testing Market, by Related Revenue, 2025

Ranking	Company	Revenue (RMB100 million)	Market Share
1	Company A	282.6	22.4%
2	Company B	196.2	15.5%
3	Company C	117.0	9.3%
4	Company D	79.5	6.3%
5	Company E	65.0	5.2%
6	Company F	26.3	2.1%
7	Company G	21.9	1.7%
8	**Our Company**	**15.8**	**1.3%**
9	Company H	14.4	1.1%
10	Company I	14.3	1.1%
	Others	429.0	34.0%
	Total	**1,262.0**	**100.0%**

Source: Annual reports of respective companies, expert interview, Frost & Sullivan

Notes:

Company A: A company listed on the main board of the Shanghai Stock Exchange, headquartered in Jiangsu Province, primarily engaged in IC packaging and testing and related technical services. Its products and solutions cover advanced packaging, wafer-level packaging, SiP, and high-performance computing chip packaging, among others.

Company B: A company listed on the main board of the Shenzhen Stock Exchange, headquartered in Jiangsu Province, primarily engaged in IC packaging and testing services. Its products and applications encompass packaging and testing solutions for network communications, AI, automotive electronics, and other fields.

Company C: A company listed on the main board of the Shenzhen Stock Exchange, headquartered in Gansu Province, primarily engaged in IC packaging and testing and related technical services. Its products and services include leadframe packaging, substrate packaging, wafer-level packaging, wafer testing, and finished product testing, among others.

Company D: A non-listed company headquartered in Beijing. It provides packaging and testing services across discrete devices, analog, radio frequency (RF), and other chip domains.

Company E: A company listed on STAR Market of the Shanghai Stock Exchange, headquartered in Jiangsu Province, primarily engaged in wafer-level advanced packaging and mid-end manufacturing services. Its products and solutions include wafer-level packaging and high-performance computing chip packaging and testing, among others.

Company F: A company listed on the STAR Market of the Shanghai Stock Exchange, headquartered in Zhejiang Province. It provides packaging and testing services with a focus on advanced packaging technologies.

Company G: A company listed on the STAR Market of the Shanghai Stock Exchange, headquartered in Anhui Province, primarily engaged in high-end advanced packaging and testing services. Its products and services cover bumping, wafer testing, and packaging and testing, among others.

Company H: A non-listed company headquartered in Guangdong Province. It is primarily engaged in IC memory chip packaging and testing and related technical services.

Company I: A non-listed company headquartered in Jiangsu Province. It is primarily engaged in IC packaging and testing and related technical services.

OVERVIEW OF GLOBAL DISPLAY DRIVER INTEGRATED CIRCUIT ADVANCED PACKAGING AND TESTING INDUSTRY

Definition of Display Driver IC Advanced Packaging and Testing

Display driver integrated circuit (DDIC) packaging and testing represents a critical stage between wafer front-end processing and user delivery, essential for ensuring chip reliability, yield, and final performance. DDIC packaging primarily employs bumping, flip chip, and wafer-level packaging technologies — qualifying it as advanced packaging. Through processes such as dicing, bonding, and molding, the processed wafers are transformed into independent chip products with circuits connected to external components. This is followed by functional and reliability verification using semiconductor testing equipment to ensure performance meets specifications.

As display technology evolves from liquid crystal display (LCD) and organic light-emitting diode (OLED) toward Active-Matrix Organic Light-Emitting Diode (AMOLED), flexible, and shaped panels, the demand for higher I/O density, smaller pad pitch, and multi-function integration in packaging and testing technologies continues to increase, driving deep technological innovation and steady market expansion in this segment.

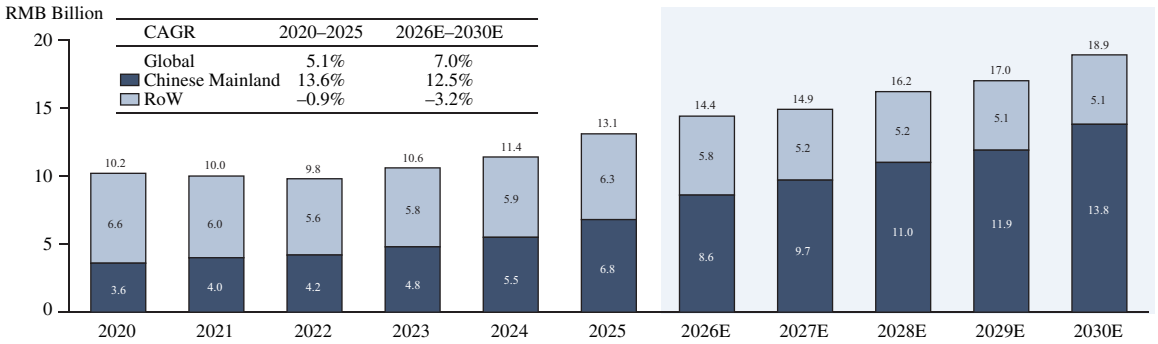
Market Size of Global and Chinese Mainland DDIC Advanced Packaging and Testing

Advanced packaging serves as a key driver for value enhancement in the DDIC market. For DDICs specifically, the pursuit of higher resolution and narrower bezels has imposed increasingly stringent requirements on packaging technologies, driving the penetration of advanced packaging

solutions. From 2020 to 2025, the global DDIC advanced packaging and testing market expanded from RMB10.2 billion to RMB13.1 billion, with a CAGR of 5.1%. The market is expected to maintain steady growth, reaching RMB18.9 billion by 2030.

In the China market, from 2020 to 2025, the Chinese DDIC advanced packaging and testing market expanded from RMB3.6 billion to RMB6.8 billion, with a CAGR of 13.6%. The market is expected to maintain steady growth, reaching RMB13.8 billion by 2030, with a CAGR of 12.5%.

Market Size of Global and Chinese Mainland DDIC Advanced Packaging and Testing, by Revenue, 2020–2030E



Source: SEMI, WSTS, Frost & Sullivan

Growth Drivers for the Global and Chinese Mainland DDIC Advanced Packaging and Testing Industry

Strong driving effect from the growing automotive chip market. The rapid growth of the automotive chip market in recent years has emerged as an important new momentum for the DDIC packaging and testing industry. Automotive chips focus on core application areas such as automotive electronic infotainment, instruments, head-up displays, smart cabins, and advanced driver assistance systems (ADAS). This market's incremental demand has driven significant structural upgrades and market expansion in DDIC packaging and testing.

Display technology iteration and upgrades promoting advanced packaging and testing technology adoption. The penetration rate of active-matrix organic light-emitting diode (AMOLED) in smartphones and wearable devices continues to increase, which has begun commercial deployment in high-end televisions and automotive displays. These new display technologies have imposed higher requirements on current accuracy, response speed, and integration density of driver chips, directly driving demand for advanced packaging and testing technologies and capacity.

Diversified expansion of downstream application scenarios. Beyond traditional consumer electronics, emerging sectors such as automotive displays, industrial control equipment, augmented reality/virtual reality (AR/VR) devices, commercial displays, and smart homes are emerging as new growth engines for DDIC demand, bringing incremental market opportunities for the packaging and testing industry.

Supply chain regionalization and self-reliance demands. Intensifying global geopolitical factors have heightened considerations around supply chain security. As the world's largest display panel manufacturer and consumer, Chinese Mainland has made domestic substitution across the entire DDIC design, manufacturing, and packaging and testing chain a clear strategic priority, providing growth momentum for local packaging and testing companies.

Development Trends in the Global and Chinese Mainland DDIC Advanced Packaging and Testing Industry

Technological advancement toward high integration and functional systematization. Packaging technology is evolving from single-driver functionality toward integrated touch, timing control, and even partial power management functions. More advanced forms such as chip-scale packaging and fan-out packaging are being explored in high-end applications.

Accelerating domestication and market share gains in the Chinese Mainland market. Leveraging advantages in geographic proximity, service responsiveness, cost control, and policy support, the Chinese mainland packaging and testing companies are capturing increasing orders from local panel and chip design companies, with market share continuously expanding and gradually covering markets traditionally dominated by Taiwan-based manufacturers.

Competitive focus shifting from capacity competition to technology and solution competition. Industry competition is progressively transitioning from pure scale and cost competition toward the ability to provide advanced packaging solutions meeting next-generation display technology requirements, conduct early-stage technology collaboration with leading chip design companies, and ensure extremely high production yield and reliability.

Increasingly close upstream-downstream strategic binding. As DDIC packaging and testing requires close alignment with chip design specifications and panel parameters, deep strategic binding between packaging and testing companies and leading chip design companies and panel manufacturers is becoming the norm, reducing R&D risks and ensuring capacity and order stability.

Competitive Landscape of the Global and Chinese Mainland DDIC Advanced Packaging and Testing Industry

As Chinese Mainland's panel display industry continues to advance supply chain localization, DDIC wafer capacity has accelerated its transfer to the Chinese mainland, driving steady expansion of the Chinese Mainland DDIC advanced packaging market. Industry-leading companies have established relatively dominant market positions through first-mover technological advantages and capacity deployment. Our DDIC advanced packaging business achieved revenue of RMB1.58 billion in 2025, with a market share of approximately 23.2%, ranking second in the industry.

Competitive Landscape of the Chinese Mainland DDIC Advanced Packaging and Testing Market, by Related Revenue, 2025

Ranking	Company	Revenue (RMB 100 million)	Market Share
1	Company G	20.1	29.6%
2	**Our Company**	**15.8**	**23.2%**
3	Company B	11.2	16.5%
4	Company J	4.7	6.9%
5	Company K	2.4	3.5%
	Others	13.8	20.3%
	Total	**68.0**	**100.0%**

Source: Annual reports of respective companies, expert interview, Frost & Sullivan

Note: Companies B and G are listed in the above table.

Company J: A non-listed company headquartered in Jiangsu. It provides advanced packaging and testing services across display driver ICs, power management and sensor chip domains.

Company K: A non-listed company headquartered in Jiangsu. It primarily engages in advanced packaging solutions for display driver IC and related applications.

Cost Structure Dynamics in the Semiconductor Packaging and Testing Market

Raw material constitutes one of the most significant cost components in the advanced packaging industry, with gold and photoresist exerting the most notable impact.

Bumping processes primarily use metal target materials, among which gold is one of the key raw materials. International gold prices fluctuated from approximately US$1,680–1,950 per ounce in 2021 to approximately US$2,600–4,300 per ounce in 2025, with price volatility further increasing in 2025. Such fluctuations were primarily driven by global macroeconomic uncertainty, geopolitical risks, rising safe-haven demand and changes in monetary policy expectations among major economies. Fluctuations in gold-related material prices may have a certain impact on raw material costs within the packaging and testing industry. On the photoresist front, constrained by the long-term dominance of core technologies held by established international suppliers, prices maintained an elevated range of approximately US$5,000–6,000 per liter during 2021–2025, representing a modest increase from the approximately US$4,500–5,500 per liter range in 2021.

Constraints and Challenges to the Industry

Increasing technical complexity. As packaging technologies continue to evolve toward higher integration density and finer interconnection pitch, packaging and testing service providers are required to continuously improve process control, yield management and reliability validation capabilities.

High capital investment requirements. Advanced packaging and testing require continuous investment in equipment, cleanroom facilities and process development. This may raise entry barriers and place higher requirements on companies' capital planning and production utilization.

Customer certification and supply chain coordination. Packaging and testing services are closely linked to chip design, wafer manufacturing and downstream application requirements. Service providers generally need to undergo customer qualification processes and maintain close coordination with upstream and downstream partners to support stable mass production.

Entry Barriers to the Industry

Technology and process barriers. Packaging and testing involve complex processes such as bumping manufacturing, high-precision testing and flip chip packaging, with high requirements for consistency and reliability despite relatively slower technology iteration. New entrants require prolonged R&D accumulation and technological breakthroughs to achieve mass production standards.

Customer certification and relationship barriers. Chip design companies and downstream customers tend to establish long-term, stable relationships with existing packaging and testing partners for collaborative technology development. New players find it difficult to gain customer trust and enter their supply chain systems in the short term.

Economies of scale and capital barriers. Building an advanced packaging and testing production line requires substantial capital investment. Meanwhile, industry profit margins are relatively limited, necessitating large-scale production to spread fixed costs and achieve profitability. This imposes extremely high requirements on new entrants' financial strength and ability to secure stable orders.

Talent and experience barriers. Process engineers, R&D experts, and quality management teams with extensive experience constitute core corporate assets. These multi-disciplinary talents are scarce and concentrated in existing leading enterprises, forming significant talent barriers.

SOURCE OF INFORMATION

For the purpose of the [REDACTED], we engaged Frost & Sullivan, an independent market research and consulting firm, to analyze the semiconductor packaging and testing market and prepare the Frost & Sullivan Report. Frost & Sullivan is an independent global consulting company

established in 1961 in New York, whose services include industry consulting, market strategy consulting, and corporate training, among others. We have paid Frost & Sullivan a fee of RMB450,000 for the market research services rendered, which we believe is consistent with prevailing market prices.

In compiling and preparing the Frost & Sullivan Report, Frost & Sullivan has conducted (i) primary research, including interviews with industry participants, competitors, downstream customers, and recognized third-party industry associations; and (ii) secondary research, including review of company annual reports, databases of relevant official institutions, and Frost & Sullivan's proprietary database accumulated over decades. Market projections in the Frost & Sullivan Report are based on the following key assumptions for the forecast period: (i) the global market's social, economic, and political conditions will remain stable during the forecast period; (ii) government policies toward the global and China semiconductor packaging and testing markets will remain consistent during the forecast period; and (iii) the semiconductor packaging and testing market will be driven by the factors described in the Frost & Sullivan Report.

Unless otherwise stated, all data and projections contained in this section are sourced from the Frost & Sullivan Report. The commissioned report was independently prepared by Frost & Sullivan and was not influenced by our Company or other stakeholders. The Directors confirm that, to the best of their knowledge after making reasonable enquiries, there has been no material adverse change in the market data since the date of the Frost & Sullivan Report that may restrict, contradict, or affect the data presented in this section.