OVERVIEW

We are a leading DRAM[(1)] chip design company in China. Leveraging our technological expertise, industry partnerships and comprehensive product portfolio, we have built a broad customer base and achieved large-scale commercialization of our products and solutions. In 2025, we sold over 100 million memory chips (including chips contained in modules and wafers). The DRAM market is generally divided into mainstream and niche segments. We focus on the niche segment, which includes 8Gb DDR4 and older generation products. Mainstream DRAM, typically characterized by its large capacity and high speed, is mainly used in standardized devices like smartphones and PCs. In contrast, niche DRAM is developed based on mature technologies and often have lower performance demands, serving specialized applications with more stable market share, accounting for approximately 7.0% of the global DRAM market and 12.3% of the Chinese DRAM market in terms of sales revenue in 2025. Please see "Industry Overview – Overview of the Global and China Niche Dram Market – Definition of Niche DRAM and Mainstream DRAM" According to Frost & Sullivan, in terms of niche DRAM revenue in 2025, we ranked fifth among Chinese companies and fourth among Chinese fabless companies in the global niche DRAM market and 12th among all players in the global niche DRAM market. We have developed expertise in Wafer-on-Wafer 3D heterogeneous integration technology and are advancing toward achieving mass production of high bandwidth memory products.

We are committed to developing high-bandwidth, low-power, and highly reliable memory solutions. Our product lineup spans multiple generations of DRAM memory types, offering comprehensive system-level memory solutions that are widely applicable in consumer electronics, network communications, automotive electronics, energy and industrial control systems. We are strategically focused on high-bandwidth and high-performance products to meet diverse market demands across various sectors. Through our independent R&D, we have developed expertise in high-bandwidth memory products. We maintain long-term partnerships with PSMC, a globally renowned wafer foundry, and have established collaborations with ADATA and Ramaxel, two of the world's top 10 DRAM module manufacturers according to Frost & Sullivan, ensuring a stable and robust supply chain. Leveraging our international R&D and sales teams, along with our Zentel brand inherited from Zentel Japan, which boasts over 20 years of history, we have developed business relationships with premium customers worldwide, enabling us to rapidly expand our customer network and tap into vast market opportunities.

Our innovation capabilities have garnered widespread recognition and respect both domestically and internationally. In 2025, we were designated as a National-Level Specialized and Sophisticated Key "Little Giant" Enterprise (國家級專精特新重點「小巨人」企業). In 2024, we were designated as a National-Level Specialized and Sophisticated "Little Giant" Enterprise (國家級專精特新"小巨人"企業), recognized as a Provincial-Level Enterprise Research Institute (省級企業研究院), awarded the Most Innovative and Dynamic Small and Medium Enterprise (最具創新活力中小企業獎) by the Zhejiang Semiconductor Industry Association (浙江省半導體行業協會), honored as a "Gold Member" of the Diversified Computing Promotion Committee by the China Communications Standards Association (中國通信標準化協會), and granted membership certificates by the Global Computing Consortium (全球計算聯盟) and the China Automotive Chip Industry Innovation Strategic Alliance (中國汽車芯片產業創新戰略聯盟). We are also actively engaged in cutting-edge industry research, with multiple collaborative papers, in partnership with academic and research institutions such as ETH Zurich, published in top-tier international conferences such as IEEE Symposium on Security and Privacy (one of the four major computer security conferences globally) and ACM/IEEE International Symposium on Computer Architecture (a leading conference in computer architecture).

Benefiting from the recent rapid expansion of the global and China memory chip and AI computing industries, we have experienced a continuous improvement in the sales of our major products. During the Track Record Period, the total storage capacity of our products sold grew from approximately 29.3 million GB in 2023 to approximately 54.3 million GB in 2025, representing a CAGR of 36.1%.

Note:

(1) "DRAM" stands for dynamic random-access memory, a type of random-access memory that requires periodic refreshing to maintain the stored information.

Our Products and Solutions

We specialize in the R&D, design and sales of DRAM chips. Our product portfolio includes DRAM chips, DRAM modules and DRAM KGD wafers, all of which have contributed to our historical success and are poised to capture significant market opportunities in the future. According to Frost & Sullivan, the global DRAM market reached RMB984.1 billion in 2025, and is expected to further expand at a CAGR of 22.3% from 2025 to 2030. In particular:

DRAM Chips: Our independently designed DRAM chips undergo rigorous packaging and testing, making them ideal for embedded systems with broad applications in both commercial and industrial sectors. Commercial-grade DRAM chips are primarily used in consumer electronics and network communications, such as robots, smart speakers, and Wi-Fi devices, while industrial-grade memory chips are tailored for demanding industrial control applications, particularly those requiring high reliability in extreme temperature environments. These chips ensure stability and longevity under extreme operating conditions.

DRAM Modules: Our DRAM modules are crafted by integrating memory chips with PCB using advanced packaging technologies. They are widely used in high-end computing products, including industrial PCs and enterprise servers. Through efficient packaging and modular design, our DRAM modules deliver exceptional performance and stability, meeting stringent requirements for storage density, speed, and reliability across diverse application scenarios.

DRAM KGD Wafers: We provide customized DRAM KGD wafers primarily for SoC manufacturers. During the chip design phase, we conduct precise wafer testing tailored to customer specifications and deliver qualified wafers to downstream manufacturers for further packaging and processing. Through deep collaboration with customers, our wafers consistently meet their high technical standards.

During the Track Record Period, our revenue amounted to RMB580.3 million, RMB646.4 million and RMB1,104.9 million, respectively.

OUR COMPETITIVE STRENGTHS

We are a Leading DRAM Chip Design Company in China with Vast Future Growth Potential.

According to Frost & Sullivan, DRAM chips are among the most widely used and standardized foundational products in the integrated circuit industry, with market demand showing considerable growth. DRAM can be broadly categorized into niche and mainstream markets based on market popularity. We specialize in the niche market, focusing on 8Gb DDR4 and earlier-generation products, primarily serving the consumer electronics and network communications, as well as automotive electronics, energy and industrial applications with small to medium-capacity storage needs. As a leading provider of DRAM solutions in China, we offer a comprehensive range of DRAM products, including DRAM chips, DRAM modules and DRAM KGD wafers, across multiple generations, and have accumulated cutting-edge technologies pertaining to the development of high-bandwidth 3D stacked memory solutions. Our extensive portfolio positions us as one of the few domestic DRAM chip design companies which possess the complete iterations of DRAM products from SDR to DDR4, capable of meeting diverse market demands across various sectors. Backed by a global team, cutting-edge R&D capabilities, and strong partnerships across the supply chain, we have established a broad and high-quality customer base, enabling large-scale product sales both domestically and globally.

According to Frost & Sullivan, the DRAM industry is poised for sustained growth, fueled by supportive government policies and the rapid expansion of downstream applications. The Chinese government has introduced a series of favorable policies, including tax incentives, digital economy development plans, and industry-finance collaboration initiatives, to support the growth of the memory chip industry. The global DRAM market has reached RMB984.1 billion in 2025, with a further 111.1% growth projected in 2026. The niche DRAM market, valued at approximately RMB68.6 billion in 2025, benefits from diversified applications, ensuring its continued market share in the DRAM market in the medium to long term. In 2025, our niche DRAM products accounted for 1.0% of the global niche DRAM market. In addition, Chinese companies generated an aggregated revenue of RMB6.3 billion in 2025 with a total market share of 9.2% in the global niche DRAM market. We accounted for 10.4% of the aggregated revenue generated by Chinese companies in 2025, ranking fifth among Chinese companies and fourth among Chinese fabless companies in the global niche DRAM market. We will continue to expand our customer base, increase our market share in the niche DRAM market, and leverage long-term R&D investments and supply chain partnerships to gain foothold into the mainstream DRAM market.

According to Frost & Sullivan, the rapid growth of AI applications, surging demand for computing power, and accelerated innovation are driving explosive growth in the high-bandwidth stacked DRAM market in China, which is expected to remain in undersupply for the foreseeable future. With deep technical expertise, strong R&D capabilities, and robust ecosystem partnerships, we are one of the few domestic memory solution providers to achieve breakthroughs in high-bandwidth stacked DRAM technology. We aim to be among the first to achieve mass production of these products, which will provide room for significant future growth. During the Track Record Period, we have achieved commercialization of our silicon interposer solutions and achieved design service and licensing fees revenue related to our AI memory-computing solutions.

As a leader in DRAM chip design, we are well-positioned to capitalize on the growing demand for DRAM chips and high-bandwidth stacked DRAM products. With strong policy support, expanding downstream applications, and a commitment to innovation, we are poised for sustained growth and market leadership in the years to come.

Our Multi-Center R&D Platform and Long-Term Technological Expertise Have Established a Mature Leadership Position in Technology.

We have established a multi-center R&D platform with research centers in both Hangzhou, China and Osaka, Japan. This international R&D network allows us to leverage the unique technological strengths of each region, attract top talent from different countries, and foster cross-regional technical collaboration, which in turn deepens our understanding of cutting-edge R&D trends both domestically and globally and enhances our overall R&D capabilities. As of December 31, 2025, we had a total of 86 R&D personnel. As of the Latest Practicable Date, we had registered 92 patents, comprising 83 in the PRC, 6 in Japan and 3 in the U.S., and 11 integrated circuit layout designs in the PRC.

Building on the experience in developing products from SDR to DDR4, we possess proprietary technologies for DRAM and memory-computing products. According to Frost & Sullivan, we are one of the few domestic DRAM chip design companies which possess the complete iterations of DRAM products from SDR to DDR4. Our extensive experience in technological iteration has enabled us to accumulate a continuous and comprehensive set of core technologies across all stages of chip development. Through targeted design processes, we are able to enhance product performance, improve yield rates, and reduce costs in testing and other key aspects. Some of the key chip design and testing technologies we have successfully implemented include ECC (error correction code) integrated circuit design, KGD (known good die) design technology, advanced-node design technology (19nm and below), and DRAM core array testing and repair technology.

Through continuous accumulation of experience in iterative research and development, we have established a two-dimension management system for product and technology development. This system features vertical collaboration between our R&D and business departments, as well as horizontal coordination among specialized R&D teams. This dynamic R&D mechanism enables us to effectively address the ever-evolving technical demands of the memory industry, significantly enhancing the predictability and efficiency of future development efforts. In addition, our comprehensive experience in technological iteration allows us to better understand and meet customer demands for diversified memory solutions, particularly in terms of response speed and efficiency. Key examples of how we leverage our technological advantages include:

- *Enhancing Product Performance through Design Improvements:* With our in-depth understanding of product technologies, we innovatively incorporate lower voltage designs to reduce power consumption, making our products compatible with various power supply conditions. Furthermore, our design improvements optimize memory arrays, effectively reducing chip size and creating a competitive edge compared to similar products. For instance, our 512Mb DDR2 product has a chip size nearly 10% smaller than comparable products from competitors using the same process.

- *Meeting Customization Needs through Technical Adaptation:* Our DRAM modules are designed to be compatible with a wide range of CPUs from mainstream domestic manufacturers, providing a solid technical foundation for customized product development. In addition, our technical expertise allows us to quickly and efficiently meet customer-specific requirements. For example, when developing ECC-equipped product with additional features such as write data masking and double-error detection alerts, we reused existing design resources to significantly shorten the R&D cycle for customized solutions.

- *Improving R&D Efficiency through Technological Accumulation:* We maximize the repeated utilization of existing designs and programming resources to shorten the time from design to testing, reduce development costs, and improve R&D efficiency. For example, during the development of a 25nm 2Gb DDR3 product, we introduced a faster and more reliable circuit verification system based on our experience with similar products, significantly shortening the R&D cycle.

According to Frost & Sullivan, high-bandwidth memory products are critical to overcoming storage bottlenecks in future AI applications and are increasingly becoming the mainstream memory solution for GPUs. We have independently developed a "1 Logic Wafer + 1 DRAM Wafer" solution based on our self-developed Wafer-on-Wafer 3D heterogeneous integration technology. This solution vertically integrates logic wafers and DRAM wafers using TSV and hybrid bonding technologies, which eliminates the need for interposers and COWOS packing, significantly reducing cost, latency and power consumption while maximizing bandwidth, resulting in a high-bandwidth 3D stacked memory solution.

As one of the few domestic companies with high-bandwidth 3D stacking technology, our advanced 3D stacking solution delivers higher performance, lower power consumption and reduced latency comparing to 2.5D stacked products. The integration of logic and DRAM wafers also ensures better compatibility with AI memory-computing requirements. Moreover, our ability to connect logic and DRAM wafers produced using different manufacturing processes allows us to efficiently design high-bandwidth memory products for large, medium, and small systems, offering exceptional design flexibility.

Our multi-center R&D platform, combined with our long-term technological expertise, has solidified our leadership in the memory and AI memory-computing sectors. By continuously innovating and adapting to market demands, we are well-positioned to maintain our competitive edge and drive future growth in the high-bandwidth memory market.

We Offer Comprehensive Memory Solutions to Meet Diverse Customer Needs.

As a leading DRAM chip design company in China, we specialize in delivering a full range of memory products and customized services. Our product portfolio currently includes DRAM chips, DRAM modules and DRAM KGD wafers, and is poised to expand with next-generation AI memory-computing solutions. Leveraging cutting-edge technology and innovative R&D capabilities, we have established a significant competitive edge in the intelligent storage sector, enabling us to fully address the diverse needs of customers across various industries.

Our DRAM chips are widely used in consumer electronics and network communications, such as robots, smart speakers, and Wi-Fi devices, as well as in automotive electronics, energy and industrial control systems. Our DRAM modules are primarily deployed in high-end intelligent products like industrial PCs and enterprise servers, meeting stringent requirements for storage density, speed, and reliability across different application scenarios. Memory wafers are tailored for SoC controller manufacturers, offering customized solutions based on customer specifications. Additionally, our AI computing-enabled memory products are designed for cutting-edge applications such as AI inference, edge computing, and autonomous driving, addressing storage bottlenecks in data-intensive AI applications while enhancing computational efficiency and integrated memory-computing performance.

With deep technical expertise and leading-edge memory product design capabilities, we are adept at flexibly meeting the diverse needs of customers across industries, providing tailored product solutions. Our product matrix encompasses a full range of DRAM products, and we are expanding into next-generation high-bandwidth memory solutions. This enables us to offer comprehensive memory solutions spanning from consumer electronics to enterprise-level applications. Our extensive product portfolio not only meets a wide range of customer needs, helping them reduce the number of suppliers and strengthen supply chain management, but also significantly enhances our competitive advantage in supplier qualification and market competition. Specifically, we have entered into a development agreement with PSMC in respect of the development of DRAM products based on 19nm and below nodes, which is a testament of our R&D prowess and our close collaboration with our production partners.

Leveraging advanced manufacturing processes and rigorous quality testing, our products deliver exceptional performance, characterized by high quality, reliability, stability, and consistency. Our commercial-grade DRAM chips are designed for standard temperature environments and comply with the international JEDEC standards, demonstrating extremely low defect rates. Our industrial-grade DRAM chips operate reliably in harsher temperature conditions while also adhering to the applicable standards. Furthermore, as a benchmark for high-specification wide-temperature applications, our automotive-grade chips perform stably under extreme temperature conditions and have successfully passed the AEC-Q100 Grade 2 certification, the highest international standard, signifying global recognition of our product quality.

Through years of product iteration and technological upgrades, we have accumulated industry-leading expertise and know-how, enabling us to deliver exceptional after-sales services. With an in-depth understanding of product technical details, we can comprehensively address potential issues customers may encounter during product usage, providing professional technical support and consulting services to ensure an optimal experience throughout the product lifecycle.

With leading design capabilities, a diverse product portfolio, product performance, and efficient after-sales services, we have earned widespread recognition in the DRAM chip industry. We have established deep partnerships with global technology leaders. Through collaborations with industry pioneers, we continuously improve our products and services, enhance our brand influence, and further solidify our leadership position in the DRAM chip industry.

We Build Scalable Commercial Capabilities Through Long-term and Stable Ecosystem Partnerships.

According to Frost & Sullivan, the DRAM chip industry is characterized by its resource-intensive nature, requiring substantial investments and increasingly specialized divisions of labor. Due to the lengthy cycles of production capacity expansion, the market exhibits periodic fluctuations in supply and demand despite its overall upward trend. This dynamic environment demands rapid adaptation to market changes, rendering it essential to maintain close collaboration across the industry chain. Chip design companies, fabrication foundries, and packaging and testing companies need to work together to address production challenges and respond promptly to market shifts. It is also through such cooperation that companies can focus their resources, expand their competitive advantages, and collectively drive the growth of the DRAM chip industry.

In terms of supply chain management, we have established close relationships with key suppliers across critical production stages. We are a long-term business partner of PSMC, one of the world's leading wafer foundries. PSMC has been manufacturing DRAM wafers for Zentel Brand for over 20 years (covering business relationship between PSMC's predecessor prior to its spun off from PIHC (formerly known as Powerchip Technology Corporation) and Zentel Japan since 2004). Through this lasting partnership, we have accumulated extensive experience in the R&D and iteration of DRAM products across different generations and processes. This has given us a profound understanding of PSMC's production workflows, process technologies and personnel, enabling us to enhance product yield and reduce production time and costs through targeted design processes and close collaboration. For instance, we have improved testing efficiency through multi-wafer parallel testing, optimized hardware designs such as probe cards and test carriers to extend equipment lifespan and reduce replacement frequency, and implemented monitoring and control of PSMC's manufacturing processes regularly. By collecting and analyzing real-time data and monitoring key metrics, we can automatically adjust parameters or detect anomalies early, thereby improving product yield. These measures require cross-departmental collaboration among chip design, equipment maintenance, and testing engineering teams to strike the optimal balance between yield improvement and cost reduction, ultimately enhancing production efficiency and product quality. We maintain close communication with PSMC to mitigate the impact of supply chain fluctuations on our inventory and supply. In addition, we collaborate with PSMC on continuous innovation and upgrades, jointly advancing the development and mass production of products with more advanced process. Apart from PSMC, we have also established partnerships with global leading DRAM module manufacturers, such as ADATA and Ramaxel, ensuring our supply capabilities in system-level storage products.

In terms of customers, we have forged strong collaborations with numerous globally renowned customers, successfully applying our products to markets such as consumer electronics, network communications, automotive electronics, power edge computing, and industrial control systems. For example, we are a major DRAM chip supplier to a global leader in computer and printer manufacturing, a leading communication equipment manufacturer in Europe, a leading router manufacturer in China, and a prominent IoT SoC chip design company in China, solidifying our market leadership. We actively seek feedback from these valuable customers to refine our products and services while meeting their diverse requirements. By providing professional technical support and consulting services, we ensure an optimal experience throughout the product lifecycle, which has been proven effective in enhancing customer loyalty.

To address evolving market trends, we are committed to expanding our collaborative ecosystem. Leveraging our leading position in the DRAM chip industry and the exceptional service experiences of our existing customers, we have successfully onboarded renowned customers such as Lenovo Kaitian, promoting the application of our products and technologies in smart TVs, media players, computers, and servers. Currently, we are focused on the R&D and market expansion of AI memory-computing solutions and have established strategic partnerships with leading AI computing chip companies in China. As our AI memory-computing solutions continue to mature, we anticipate more diverse commercial applications in the AI sector addressing the different evolving needs of our customers.

Finally, we strive to build long-term partnerships with global premium customers through high-quality products and services. Our goal is to align our product development direction with the strategic objectives of our customers, with comprehensive support and interactions with our premium customers, thereby creating shared value and fostering mutual growth.

We Boast a World-class Customer Portfolio and Continue to Expand Our Presence in International Markets.

Leveraging years of R&D experience and intellectual property accumulation, we have developed expertise in a range of technologies and know-how, from product design and verification testing to quality control and mass production. Over the years, we have built a solid foundation and business partnerships with over 100 global customers. Our strategic sales network combines both distributor and direct sales models to serve markets worldwide. Distributors enable us to reach customers efficiently, while direct sales foster close collaboration, allowing us to provide real-time support, in-depth technical assistance, and long-term customer relationships. To date, we possess the technical expertise, extensive industry experience, and strong reputation needed to serve global industry leaders, with our capabilities and market position widely recognized by our customers.

According to Frost & Sullivan, in the memory industry, leading customers impose stringent supplier qualification processes, creating high entry barriers. DRAM design, in particular, involves balancing storage density, speed, power efficiency and stability, resulting in significant technical challenges and a limited number of specialized DRAM design companies. Given the long product lifecycles and strict stability requirements in our sector, close technical collaboration with customers during the R&D phase is essential. Our deep technical expertise allows us to systematically support customers throughout product development. With a top-tier service team, we assist customers in interference resistance verification and reliability testing, therefore ensuring superior product performance. Our strong technical capabilities and exceptional service enable us to precisely understand customer needs, penetrate target markets, and co-develop high-quality solutions with industry leaders. Our end customers span a wide spectrum of industries, including Fortune 500 companies or Top 500 Chinese Enterprises in printer manufacturing, router manufacturing, networking equipment and IoT SoC design. Being selected as a supplier by these major corporations not only validates our product excellence and R&D prowess but also serves as a key driver for our future growth.

We have successfully diversified our product applications across multiple markets, including consumer electronics, network communications, automotive electronics, power edge computing, and industrial control systems. For example, according to Frost & Sullivan, we are a leader in the niche DRAM market, with our DDR3 products capturing considerable market share in the Chinese telecommunication operator market for WiFi6 & GPON. We have also made breakthroughs in the domestic IT application innovation sector, notably securing memory supply contracts for several leading Chinese communication equipment manufacturers. Currently, we are focused on developing and commercializing AI memory-computing solutions, collaborating with over 20 partners, including (i) Enrigin Technology Co., Ltd. ("**Enrigin**"), which is a leading AI computing chip company, (ii) a high-performance heterogeneous AI computing chip innovator in China and (iii) a premier CPU developer in China. As our AI memory-computing solutions mature, we anticipate broader commercialization in AI-driven applications.

According to Frost & Sullivan, the global DRAM market is projected to grow at a CAGR of 22.3% from 2025 to 2030, reaching RMB2,693.2 billion by 2030. We are actively extending our domestic strengths into overseas markets. With an international R&D center and localized sales and engineering support in key regions, we have established a strong presence in Japan, Europe and other major markets. Our overseas network enables deep collaboration with existing customers, ensuring efficient delivery while also driving steady growth through new customer acquisition. We are confident that our industry leadership, first-mover advantage, and trusted partnerships will sustain our rapid growth and unlock long-term opportunities in global markets.

Our Management and Core Team Possess Profound Technical Expertise and Extensive Industry Experience.

Our management and core team bring deep industry expertise and a wealth of technical knowledge. Mr. Ying Wei (應偉), our Chairman and non-executive Director, leverages his extensive background in investment and keen market insights to guide our Company in formulating visionary and detailed long-term development strategies. Under his leadership, our Company has successfully navigated multiple strategic transformations and phases of business expansions. Mr. Ying has provided robust support in strategic planning, resource allocation and capital operations, all contributing to our continued success. Mr. Yu Xiao (于曉), our executive Director and general manager, previously served as senior vice president at Xi'an UniIC, bringing rich management and operational experience that has significantly enhanced our operational efficiency and market competitiveness. Mr. Lin Kuo Hsiung (林國雄), our Vice Chairman and executive Director, served as vice president at Zentel Electronics Corp. and AP Memory Technology Corporation before joining our Company. His extensive industry experience has laid a solid foundation for our business expansion. Our core management team possesses profound insights into global industry trends and customer needs, enabling them to steer our Company toward fast growth, as evidenced by our past business and financial performance. For details on the biographies of our Directors and senior management, please see "Directors and Senior Management" in this document.

We boast an experienced R&D team that provides strong technological support for our consistent growth and expansion. Mr. Kim Joonho, head of our R&D department in Hangzhou, previously held key positions at SK Hynix, Infineon Technologies, and Winbond Electronics, with approximately 30 years of DRAM design and management experience. Mr. Kubo Takashi, the director of our R&D center in Japan, previously served as a senior engineer at Mitsubishi Electric and Renesas Electronics, overseeing process development and mass production for multiple products, with more than 25 years of DRAM R&D experience. Most of our core technical personnel come from renowned semiconductor companies such as SK Hynix, bringing years of relevant industry experience. As of December 31, 2025, the R&D department accounts for approximately 53.4% of our workforce, with all the R&D personnel holding bachelor's degrees or higher. They play a pivotal role in driving product innovation, enhancing production efficiency, and ensuring product quality.

We adhere to a people-centric talent management philosophy, placing huge emphasis on team motivation and management. We are committed to offering competitive remuneration packages and multi-dimensional incentives. We have established a comprehensive incentive system that offers additional bonuses for timely completion of product development and patent inventions, fostering enthusiasm and innovation within the R&D team. Through the implementation of equity incentive plans, we align the interests of core technical personnel with our Company's long-term development, thereby boosting employee motivation and reducing turnover rates.

OUR DEVELOPMENT STRATEGIES

We will Continuously Focus on Technological Innovation to Lead Transformation in Global DRAM and Memory-Computing Solutions.

To strengthen our leadership in the memory solutions sector, we are committed to ongoing R&D investments, technological innovation, and expansion of our product portfolio. In response to rapidly evolving technologies and processes in the field of DRAM and memory-computing solutions, we aim to deepen our expertise in DRAM product manufacturing, enhance product performance, and build technical barriers to solidify our competitive edge. By overcoming existing product limitations, we strive to lead the global transformation in DRAM and memory-computing solutions. Specifically:

- *Advancing high-bandwidth memory technology:* We will continue to invest in the development of high-bandwidth memory products, focusing on the implementation of 3D heterogeneous integration solutions. By combining 2D and 3D stacking technologies, we aim to develop next-generation solutions that will solidify our technological leadership in DRAM and memory-computing fields.

- *Upgrading DRAM Product Technology:* We are committed to enhancing DDR product performance by improving design processes to achieve lower power consumption and higher speeds, thereby enabling continuous organic product upgrades.

- *Progressing the development of advanced process product technologies:* We are working closely with our wafer fabrication partners to jointly progress the design of advanced process products. We will continue to invest in advanced process technology development to ensure the competitiveness of our future products.

We Will Expand Our Product Portfolio and Strengthen Our Customization and Independent Development.

Through years of dedicated R&D, we have built a diverse product matrix and are actively developing high-bandwidth memory solutions. To further solidify our leading position in the DRAM chip industry, we will continue to drive technological innovation and product iteration, with emphasis on customization and independent development to ensure each product maintains long-term competitive advantages in the market. Specifically:

- *DRAM chips and DRAM modules:* By leveraging our sophisticated R&D teams and advanced manufacturing processes, we manage to continuously improve the performance of our DRAM chips and DRAM modules. Building on our existing DRAM products, we are developing higher-capacity, higher-power-efficiency solutions to meet growing market demands and reinforce our industry leadership.

- *AI memory-computing solutions:* In the high-bandwidth memory field, we are developing leading HSM1 product and aiming for mass production by 2026. In addition, we are proactively working on the development of more advanced HSM2 product to secure a technological edge in in the ever-growing market in the future.

Through precise strategic planning and sustained R&D investment, we aim to launch a series of industry cutting-edge products, strengthen our independent R&D and customization capabilities, and enhance our market position and brand influence in the memory sector, which in turn will drive our continuous business growth and long-term development.

We Will Selectively Pursue Strategic Collaboration, Investment and Acquisition Opportunities to Integrate Industry Resources.

We plan to progressively enhance our industry chain integration by selectively pursuing strategic collaboration, investment and acquisition opportunities. We aim to accelerate our high-bandwidth memory strategy through mergers and acquisitions, by targeting primarily companies with leading in-memory processing technologies or commercialized applications. This will help us integrate internal research with external investments to expedite AI computing product development and application innovation.

We currently operate a testing facility in Jinhua, Zhejiang and plan to further strengthen our product testing capabilities. In addition, we intend to expand our packaging and testing capacity within the industry chain and explore investments or acquisitions to ensure stable and efficient production. Building on our strategic partnerships with AI computing chip companies, we will continue to strengthen our R&D capabilities and industry chain collaborations to promote increasingly extensive adoption and long-term development of AI memory-computing products.

We Will Relentlessly Implement Our Global Strategy.

With a solid customer base worldwide, we will deepen collaborations with existing customers while actively pursuing a global strategy. We aim to build and enhance our global sales network, expand into multiple regional markets, and further promote our products internationally.

We plan to strengthen our overseas sales and engineering support teams to improve customer retention. By identifying and partnering with potential distributors worldwide, we will leverage our advanced products to establish business relationships and unlock new market opportunities. We will expand local marketing and engineering support teams in key international markets and invest in localized marketing activities to cater to specific regional needs and preferences. Specifically, we will recruit additional sales and marketing personnel for our overseas sales and marketing teams. We will also strengthen our domestic sales teams to cover domestic regional markets, as well as major customers and innovative product markets.

We are committed to integrating global supply chain resources to improve delivery capabilities, enabling faster product launches and quicker responses to international customer demands. This approach will strengthen customer partnerships, provide more customized and high-quality services, and attract top global talent. It will also enhance our R&D capabilities, foster new international partnerships, and elevate our brand's global recognition.

For further details, please see "Future Plans and Use of [**REDACTED**]" in this document.

OUR BUSINESS MODEL

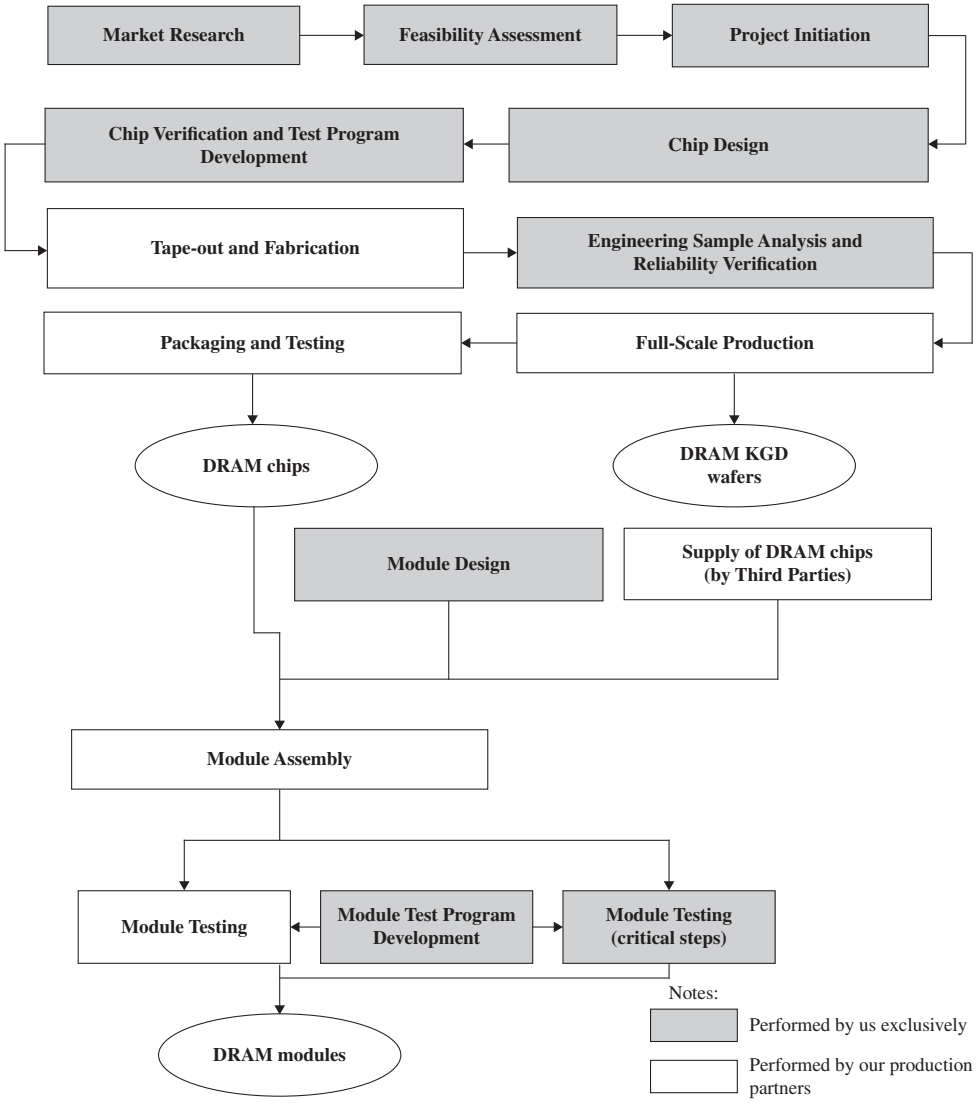
We are primarily engaged in the design and sales of DRAM products. According to Frost & Sullivan, in terms of niche DRAM revenue in 2025, we ranked fifth among Chinese companies and fourth among Chinese fabless companies. Our core competency lies in semiconductor design, encompassing the development of specialized DRAM chips and modules tailored to specific applications and market needs, and our products and solutions typically offer competitive advantages in terms of speed, power efficiency, and reliability. Based on market popularity and application scope, DRAM market can be categorized into mainstream and niche segments. We specialize in the niche DRAM market, which currently includes 8Gb DDR4 and lower-generation products. We offer a complete suite of memory solutions tailored for a wide array of applications, including consumer electronics and network communications such as Wi-Fi routers and smart home appliances, IoT devices, as well as automotive electronics, energy and industrial control equipment.

Under our fabless model, we collaborate with third-party semiconductor foundries with manufacturing capabilities, which handle the fabrication, testing, and packaging of semiconductor components based on our design specifications and requirements. This approach allows us to concentrate on our core competencies in innovation and product design, while leveraging the specialized expertise of industry-leading manufacturers for wafer fabrication, packaging, and testing. Our primary fabrication partner, PSMC, is the largest pure-play DRAM foundry based in Taiwan and one of the largest commercial DRAM foundries worldwide in terms of production capacity. PSMC handles the intricate process of wafer fabrication, which involves transforming raw materials into high-performance semiconductor wafers. Following fabrication, the wafers are delivered to DRAM packaging and testing service providers, where they undergo assembly, rigorous testing, and quality assurance processes to ensure they meet our specifications.

In terms of sales and marketing strategy, we employ a combination of direct sales and distributorship model. Under our direct sales approach, we leverage our dedicated sales team to engage with customers across various industries, including consumer electronics, network communications, automotive electronics, power edge computing, and industrial control systems. We also have an extensive network of distributors for the sales of our products. This approach allows us to efficiently manage payment term risks, reduce cash flow pressures, and gain logistical support, while also enabling us to rapidly establish regional sales networks and enhance market penetration. To ensure effective management, distributors report end customer information to us, including sales data, project details, and shipping addresses. This enables us to monitor actual sales, track logistics, and mitigate risks such as channel stuffing and cannibalization among distributors.

We apply strict quality control standards and have implemented various quality control checks to ensure that our products meet our customers' expectations and international and industry standards. We also require our business partners, including wafer manufacturer, packaging and testing service providers, assembly service providers, and delivery service companies, to apply their stringent quality control standards and meet our internal requirements. In particular, we cooperate closely with PSMC for wafer fabrication as wafer fabrication requires highly advanced technologies and PSMC is a global leader in wafer fabrication which has stringent quality standards that safeguard the quality of wafers we use for our chips.

Set forth below is a diagram which illustrates our business model:



For details of the design process, please see "Research and Development — Our Design Process" in this section. Take our DRAM chips as an example: (1) *Market Research:* Our teams analyze customer needs, market trends, and competitive landscapes to define product specifications and assess market potential; (2) *Feasibility Assessment:* Our R&D team evaluates technical feasibility, resource requirements, and potential risks, producing a detailed report for cross-functional review; (3) *Project Initiation:* A formal report summarizing market potential, technical viability, and financial projections is prepared and approved by management; (4) *Product Design:* Our R&D team develops the chip architecture and circuitry, ensuring manufacturability and performance through simulations and verification; (5) *Design Verification and Test Program Development:* The design undergoes rigorous verification, and test programs are developed to validate functionality against specifications; (6) *Tapeout and Wafer Fabrication:* The verified design is sent to the foundry for mask creation and wafer fabrication, with initial testing conducted on the first silicon; (7) *Engineering Sample Analysis and Reliability Verification:* Functional and reliability tests are performed on engineering samples, with customer feedback used for refinements if needed; (8) *Full-Scale Production:* After validation, the product enters risk production and then full-scale manufacturing, ensuring high yield and reliability; (9) *Packaging and Testing:* The final product is packaged and subjected to comprehensive testing to ensure it meets all quality and performance standards.

OUR PRODUCTS AND SOLUTIONS

As a leading provider of DRAM products in China, we offer a comprehensive portfolio of products designed to meet the diverse needs of our customers. Our product matrix spans the full range of DRAM products, including (i) DRAM chips, (ii) DRAM modules and (iii) DRAM KGD wafers, enabling us to deliver end-to-end memory solutions for applications ranging from consumer electronics to enterprise-level systems. With continuous product iteration and flexible customization capabilities, our DRAM products have rapidly expanded into various fields, including robots, smart speakers, Wi-Fi, security applications, personal computer workstations, and servers. We are also developing a range of AI memory-computing solutions which include notably cutting-edge high-bandwidth memory products which are expected to address storage bottlenecks in data-intensive AI applications, enhancing computational efficiency and enabling integrated storage and computing capabilities.

We focus on the niche DRAM market which has distinct product performance characteristics, stable downstream demand, and strong irreplaceability. According to Frost & Sullivan, the global niche DRAM market size reached RMB68.6 billion in 2025 and is expected to grow further at a CAGR of 14.7% from 2025 to 2030, reaching RMB136.2 billion by 2030, whereas the niche DRAM market size in China (including Hong Kong, Macau and Taiwan) reached RMB41.6 billion in 2025 and is expected to record a higher CAGR of 18.2% from 2025 to 2030, reaching RMB95.7 billion by 2030.

Along with the recent growth of the global and China (including Hong Kong, Macau and Taiwan) DRAM and AI computing-related industries, we have seen an overall increase in both the volume of our products sold and revenue generated from such sales. During the Track Record Period, the total storage capacity of our products sold grew from approximately 29.3 million GB in 2023 to about 54.3 million GB in 2025, representing CAGR of 36.1%. Our revenue increased from RMB580.3 million in 2023 to RMB1,104.9 million in 2025.

The following table sets forth our revenue breakdown by business segments during the Track Record Period:

	For the year ended December 31,					
	2023		2024		2025	
	RMB'000	*% of revenue (%)*	*RMB'000*	*% of revenue (%)*	*RMB'000*	*% of revenue (%)*
DRAM chips	484,164	83.5	454,391	70.2	607,824	55.1
DRAM modules	47,283	8.1	137,467	21.3	429,012	38.8
DRAM KGD wafers	47,081	8.1	54,028	8.4	46,642	4.2
AI memory-computing solutions and others[(1)]	1,818	0.3	515	0.1	21,411	1.9
Total	**580,346**	**100.0**	**646,401**	**100.0**	**1,104,889**	**100.0**

Note:

(1) During the Track Record Period, our revenue from AI memory-computing solutions and other business comprised (i) design services and (ii) royalty fees, both mainly in relation to our high-bandwidth memory products.

The following table sets forth the number and total storage capacity of our products sold during the Track Record Period:

	For the year ended December 31,		
	2023	2024	2025
Number of chips (including chips contained in modules and wafers) sold (million)	112.5	101.5	109.7
Total storage capacity sold (million GB)	29.3	34.2	54.3

Leveraging our R&D innovation and continual iterations and refinement on our products, our products consistently deliver industry-leading performance, high reliability, stability and uniformity. Below is a detailed overview of our product offerings and their unique features:

DRAM chips

Our core business focuses on the design of DRAM chips serving the niche market. A DRAM chip is a type of volatile memory chip that stores each bit of data in a separate capacitor within an integrated circuit. Since capacitors leak charge, DRAM requires constant refreshing to maintain data, thus giving rise to its "dynamic" nature. DRAM chips are widely used in computing systems due to their high density and relatively low cost compared to other volatile memory types like SRAM. They are the primary memory technology in devices such as PCs, servers, and smartphones, providing the working memory needed for running applications and processing data.

Our self-developed DRAM chips are manufactured by our fabrication partner which we have long-established business relationship, and are rigorously packaged and tested to ensure superior performance across a wide range of applications. These chips are subject to stringent quality control and available in commercial-grade and industrial-grade variants, each designed to meet specific environmental and operational requirements.

1. Commercial-Grade DRAM Chips

Our commercial-grade DRAM chips have applications across consumer electronics and network communications, such as robots, smart speakers, and Wi-Fi systems. The operating temperature ranges from 0°C to 95°C. They are compliant with mainstream international JEDEC standards. Optimized for high performance and energy efficiency, these chips are ideal for modern smart devices, ensuring seamless operation and enhanced user experiences.

2. Industrial-Grade DRAM Chips

Our industrial-grade DRAM chips have application across industrial control systems, security systems, and other high-reliability applications. The operating temperature ranges from -45°C to 125°C. They are compliant with JEDEC standards. These chips are engineered to deliver exceptional stability and longevity, making them suitable for demanding operating conditions. In particular, they are specifically designed to meet the stringent reliability requirements of industrial control applications, ensuring stable performance even in extreme temperature environments.

The following table sets forth our revenue breakdown by commercial-grade and industrial-grade variants during the Track Record Period.

	For the year ended December 31,					
	2023		2024		2025	
	RMB'000	*% of revenue (%)*	*RMB'000*	*% of revenue (%)*	*RMB'000*	*% of revenue (%)*
Commercial-grade	472,916	97.7	443,693	97.6	587,363	96.6
Industrial-grade	11,249	2.3	10,698	2.4	20,461	3.4
Total	**484,164**	**100.0**	**454,391**	**100.0**	**607,824**	**100.0**

In June 2025, we commenced the mass production of our LPDDR4 DRAM chip, which represents a significant upgrade over its predecessor. According to Frost & Sullivan, LPDDR4 is a mainstream low-power memory widely used in smart terminals and highly integrated devices. Compared to our pre-existing products, LPDDR4 DRAM chip features lower power consumption, a smaller size, and more advanced process technology, along with higher capacity and improved power efficiency. As a result, LPDDR4 DRAM chip offers better overall system performance in end customers' products and thus broader adoption across various mobile devices. In addition, our 8Gb DDR4 DRAM chip that we have previously developed has entered mass production as part of our IPTV project, further expanding its commercial deployment.

According to Frost & Sullivan, the market size of LPDDR4 grew from RMB3.7 billion in 2021 to RMB5.2 billion in 2025, and is expected to reach RMB10.8 billion by 2030. The global market size for 8Gb DDR4 products increased from RMB21.7 billion in 2021 to RMB27.9 billion in 2025. Due to its continued widespread application in general computing, servers, and industrial terminals, its market size is projected to reach RMB30.5 billion by 2030. We believe our products that have entered mass production recently are well-positioned to capture the growing downstream market demand. According to Frost & Sullivan, demand for DRAM products continues to increase and may outpace supply in certain segments. LPDDR4 and 8Gb DDR4 products have already achieved broad adoption across a range of downstream applications, demonstrating both technical qualification and market recognition. Our new LPDDR4 further improves upon its predecessor with clear performance advantages. Additionally, our products that have entered mass production recently are mainly used in IPTV devices, a sub-market experiencing rapid growth driven by advances in network and display technologies, according to Frost & Sullivan. With mass production of our new products, we are well-positioned to support the near-term customer volume ramps.

DRAM Modules

A DRAM module is a physical assembly that integrates multiple DRAM chips onto a PCB to provide a standardized memory solution for electronic devices. Common types of DRAM modules include DIMMs for desktops and servers, and SODIMMs for laptops and compact devices. These modules connect to the motherboard via slots and work together to deliver the required memory capacity and bandwidth for the system. DRAM modules simplify the process of upgrading or replacing memory in devices, making them a key component in modern computing.

Our memory module products feature meticulously designed circuit layouts and precision surface-mount manufacturing, and have undergone rigorous product and system testing. These modules primarily address the mainstream market and are widely used in high-end intelligent products, such as industrial high-performance PCs, data centers and enterprise-level servers, which are key products in the IT application innovation industry currently under rapid development.

According to Frost & Sullivan, the development of IT application innovation industry is aimed at addressing long-term overseas supply chain dependencies by establishing China's own IT foundation, encompassing domestic alternatives for CPUs storage and database services, etc.

Our DRAM modules are capable of delivering superior data transfer speeds, high storage density and stable performance under demanding conditions. The modular design facilitates easy integration into various systems, providing flexibility for diverse application scenarios. During the Track Record Period, we procure the majority of DRAM chips used in DRAM modules from third party suppliers, mainly because our DRAM modules are used in mainstream markets such as desktop computers, laptops and data centers, while our self-developed DRAM chips are positioned in niche markets, and we have not yet entered the mainstream DRAM market segments. During the Track Record Period, we mainly procured mainstream DRAM chips from (a) a leading Chinese DRAM manufacturer and (b) a Chinese subsidiary of a leading international memory chips manufacture, who mainly engages in manufacturing, assembly and testing memory chips in the PRC.

We are actively expanding our presence in the DRAM module market and have become a supplier to leading domestic computer and server manufacturers such as Lenovo Kaitian.

DRAM KGD Wafers

A DRAM KGD wafer is a thin slice of silicon on which multiple DRAM dies are fabricated simultaneously. The wafer undergoes a series of complex semiconductor manufacturing processes, including photolithography, etching, and doping, to create the intricate circuitry of DRAM dies. Each individual die on the wafer undergoes rigorous testing to identify KGD, Known Good Die — die that is fully functional and verified. Once qualified, the entire wafer containing these KGDs is delivered to our customer as a product. Customers can then dice the wafer and package the DRAM dies or integrate them into multi-chip modules, SiP, and other advanced packaging solutions, enabling flexibility for various applications and ensuring reliability in applications like chip stacking or heterogeneous integration.

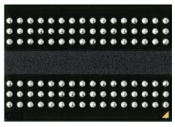
We provide customized DRAM KGD wafer solutions tailored to the needs of SoC manufacturers. Our wafers are designed and tested to meet the highest technical standards, ensuring optimal performance for downstream packaging and processing. In terms of technical design, our wafer products are primarily used for joint packaging by connecting two KGD wafers before encapsulation into a single chip, which requires compatibility of the pin designs of the two wafers or co-design of the RDL. Such design generally helps reduce costs for chip companies, according to Frost & Sullivan. In terms of customization, we are capable of precision testing and optimization based on customer requirements. We tailor parameters such as density, bandwidth, latency, and voltage to seamlessly integrate with the SoC's architecture. Each wafer undergoes rigorous testing to ensure compliance with customer specifications. Throughout the process, we work closely with our customers to deliver solutions that align with their technical and operational goals. For example, we developed a 512Mb DDR2 KGD product to meet our customers' demand for memory-integrated main chips, where the process technology improved from 38nm to 25nm, resulting in both size reduction of the product and cost reduction for our customers.

Representative Product Portfolio

Our representative products for DRAM chips include SDR/DDR series, DDR2 series, DDR3 series and DDR4 series products. DRAM modules include DDR3 UDIMM 2Rx8, DDR4 UDIMM 1Rx8, DDR5 UDIMM 1Rx8 and DDR5 RDIMM 2Rx4. DRAM KGD wafers include DDR2 KGD series and DDR3 KGD series. The table below provides an overview of some of our representative products for each of our three main product lines, including product images, features and applications:

DRAM chips

DDR3 series

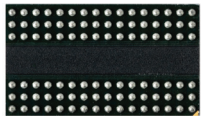


Capacity	1Gb~8Gb
Bit width	x16/x8
Working voltage	1.35V/1.5V
Operating temperature	0~95°C/-40~95°C
Package	BGA96ball/BGA78ball
Product standard	JEDEC standards
Rate	Maximum frequency of 2133Mbps (backward compatible)
Application scenarios	Network communications, ubiquitous power IoT, industrial control, set-top boxes

Product features

- High performance, high reliability
- Lightweight, low power consumption
- Ability to adapt to harsh environments
- Customized Services
- Supports industrial wide-temperature range

DDR4 series



Capacity	4Gb~8Gb
Bit width	x16/x8
Working voltage	1.2V
Operating temperature	0~95°C/-40~95°C
Package	BGA96ball/BGA78ball
Product standard	JEDEC standards
Rate	Maximum frequency of 3200Mbps (backward compatible)
Application scenarios	Network communications, ubiquitous power IoT, industrial control, set-top boxes

Product features

- High performance, high reliability
- Lightweight, low power consumption
- Ability to adapt to harsh environments
- Customized Services
- Supports industrial wide-temperature range

DRAM modules

DDR4 UDIMM 1Rx8

Capacity	8GB
Interface	DDR4 UDIMM
Temperature range	Commercial standard (applicable to ambient temperature range of 0-85°C)
Voltage	1.2V
Rate	3200MHZ, compliant with JEDEC standards
Application scenarios	Desktop, workstation, etc.
Features	A domestic module brand based on our or third parties' chips.

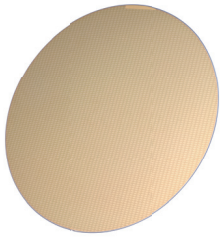
DDR5 UDIMM 1Rx8

Capacity	16GB
Interface	DDR5 UDIMM
Temperature range	Commercial standard (applicable to ambient temperature range of 0-85°C)
Voltage	1.1V
Rate	5600MHZ, compliant with JEDEC standards
Application scenarios	Desktop, workstation, etc.
Features	A domestic module brand based on third parties' chips.

DDR5 RDIMM 2Rx4

Capacity	64GB
Interface	DDR5 RDIMM
Temperature range	Commercial regulations (applicable ambient temperature range 0~85°C)
Voltage	1.1V
Rate	5600MHZ, JEDEC standards
Application scenarios	Desktop, data centers, etc.
Features	A domestic module brand based on third parties' chips.

DRAM KGD wafers



	DDR2 KGD series	DDR3 KGD series
Capacity	128Mb~1Gb	1Gb~4Gb
Bit width	x16	x16
Working voltage	1.8V	1.35V/1.5V
Operating temperature (Tj)	-25~125°C	-25~125°C
Product standard	JEDEC standards	JEDEC standards
Application scenarios	Cameras, network communications, T-CON	Network communications
Product features	• Dual channel mode • Prefetching technology • Ability to adapt to harsh environments • Customized services	• High performance, high reliability • Lightweight, low power consumption • Ability to adapt to harsh environments • Customized services

Key technologies

Below are some of the key technologies relating to (i) chip design and (ii) DRAM testing that we have developed which aim to enhance the reliability and performance of our DRAM products and provide flexible and effective solutions for fault detection and repair, ensuring our products meet the stringent demands of various high-reliability application with high efficiency:

Technologies relating to chip design

1. ECC (Error Correction Code) Integrated Circuit Design Technology

Leveraging our technical expertise across disciplines, we have successfully integrated ECC verification circuits in the DRAM chip design process. This integrated ECC technology significantly improves fault tolerance and data transmission reliability, particularly in challenging environmental conditions. Our ECC-enhanced DRAMs maintain stable operation across an extended temperature range of -40°C to 125°C or beyond, ensuring robust performance in high-stress environments.

These capabilities make our ECC-enabled DRAMs ideal for mission-critical applications that demand ultra-high reliability, such as automotive systems (ADAS, infotainment, and engine control units) and industrial automation (robotics, PLCs, and harsh-environment sensing). By mitigating soft errors and enhancing signal integrity, our technology extends product lifespans while reducing system-level failure risks.

2. KGD (Known Good Die) Design Technology

Leveraging our extensive chip design expertise and deep understanding of customer requirements, we collaborate closely with customers to develop customized KGD solutions tailored to their SoC specifications, including form factor, pin layout, operating voltage, and target speed. By integrating KGD with the customer's SoC using SiP technology, we create compact, high-performance functional modules that minimize footprint, reduce package count, accelerate testing, and enhance overall system performance.

To ensure high quality products, we implement rigorous wafer-level KGD testing protocols to validate die functionality for bare-die applications. Only products that pass our stringent wafer-level tests and meet all predefined parametric benchmarks qualify for inclusion in our KGD portfolio.

During the Track Record Period, our KGD solutions were widely adopted in security surveillance, networking equipment, and other fields. Supporting DDR2, DDR3, and other series, our products operate at voltages as low as 1.1V, offer capacities up to 4Gb, and deliver speeds up to 1,866Mb/s, addressing diverse market needs.

3. Advanced-Node Design Technology (19nm and below)

To meet growing demands for higher speeds and lower operating voltages in field applications, we partnered with PSMC in April 2025 in respect of the development of DRAM products based on 19nm and below nodes. This technology also serves as a critical foundation for our Wafer-on-Wafer DRAM stacking applications and next-generation high-bandwidth memory products, positioning us at the forefront of high-performance memory innovation.

Technologies relating to DRAM testing

1. DRAM Core Array Testing and Repair Technology

We utilize a pre-designed MBIST engine to thoroughly test the DRAM core array. When the MBIST detects a fault, the system can initiate a fault unit program to replace the damaged address with a pre-designed redundant array. This ensures thorough testing of the DRAM core array. It also supports both temporary repairs to verify the effectiveness and permanent repairs by fusing pre-designed fuses, and therefore offers flexible repair options. This technology is essential for high-reliability applications where fault tolerance and repair capabilities are critical, such as in servers and data centers.

2. Interface Interconnect Channel Testing and Repair Technology

We implement boundary scanning to test the interconnection between the host ASIC and DRAM without running the DRAM core, detecting static faults. Additionally, this technology allows us to initiate loopback testing to detect interface-related faults when the interface operates at target speeds. Therefore, it is capable of detecting both static and dynamic faults in the interface. When faults are detected, the system can initiate an interconnect channel remapping function, using pre-designed redundant I/O channels to replace damaged ones. This supports both temporary remapping to verify the repair and permanent remapping by fusing pre-designed fuses. As such, this technology is crucial for high-speed data transmission applications, such as networking equipment and high-performance computing systems.

Our Design Process

Our design process is mainly managed by the project director from our R&D teams. It is a structured and collaborative process involving multiple departments that transforms market insights and customer requirements into high-quality products. Once feasibility assessment and detailed specifications have been formulated and approved, detailed design process will commence, where architecture and circuit development are meticulously executed. Rigorous design verification ensures functionality and performance before tape-out and wafer fabrication. Engineering samples are then analyzed, and reliability is verified through extensive testing. The below illustrates the key phases of our design process:

1. Market Research. Our marketing and sales teams conduct in-depth market research to gather customer requirements, product specifications, and emerging market trends. We analyze the total addressable market, estimate potential market share, and evaluate the competitive landscape. Additionally, we assess the required investment, resource allocation, and expected return on investment. This comprehensive analysis ensures a clear understanding of market demand and opportunities, forming the foundation for informed decision-making.

2. Feasibility Assessment. Based on the insights from market research, our R&D team evaluates the technical feasibility of the proposed product. This includes assessing architecture design, process technology, potential challenges, and resource requirements. The feasibility assessment, typically completed within one month, results in a detailed report outlining design options, risks, and resource needs. This report is reviewed by cross-functional teams (marketing, sales, product engineering, quality, and operations) for approval before proceeding to the next phase.

3. Project Initiation. Once feasibility is confirmed, a formal project initiation report is prepared, summarizing market potential, technical viability, and financial projections. This report is presented to management for approval. Upon approval, the project is officially launched, and resources are allocated to move into the design phase.

4. Product Design. Our R&D team begins the chip design process, which varies in duration depending on the complexity of the technology. For mature process technologies and conventional functions, the design phase typically takes six months, while new process technologies with new functions may require up to one year. During this phase, the team focuses on architecture development, circuit design, and simulation. Before finalizing the design, a comprehensive review is conducted to ensure design verification, testability, manufacturability, and simulation results meet all requirements. Any identified issues are addressed, and the design is finalized for tapeout.

5. Design Verification and Test Program Development. The finalized design undergoes rigorous verification to ensure functionality and performance. Simultaneously, test programs are developed to validate the design against predefined specifications. This phase ensures that the chip meets all technical and quality standards before proceeding to fabrication.

6. Tape-out and Wafer Fabrication. The verified design is submitted to the foundry for mask creation and wafer fabrication. This process typically takes five months. The first batch of wafers is produced and sent for initial testing to ensure the design translates accurately into physical silicon.

7. Engineering Sample Analysis and Reliability Verification. Functional testing is conducted on the first silicon, and engineering samples are provided to customers for evaluation. Concurrently, comprehensive reliability tests (e.g., temperature, voltage, and lifespan testing) are performed to ensure the product meets stringent quality standards. Feedback from customers and internal testing is used to refine the design if necessary.

After successful validation and reliability verification, the product enters risk production to analyze yield, process stability, and reliability. Full-scale production begins once all customer and internal requirements are met. After full-scale production, the fabricated wafers are cut into individual chips, which are then packaged into the final product form. Once packaged, the chips undergo rigorous testing to verify functionality, performance, and reliability. For details of the packaging and testing process, please see "Production and Procurement — Arrangements with Our Production Partners — Packaging and Testing" in this section.

We endeavor to incorporate customer feedback and adapt to changing requirements during the design process. At each stage of the design process, there are well-defined checkpoints to evaluate our progress. If customer requirements change, the project may be modified or terminated. For customized products, we typically require our customers to commit upfront funding to cover development costs. If a project is terminated, resources are reallocated to other high-priority projects.

PRODUCTION AND PROCUREMENT

Our Fabless Model

Our company operates under a fabless business model, which means we focus exclusively on the design, development, and sales of DRAM chips while outsourcing the manufacturing processes to production partners. This approach allows us to concentrate on our core competencies in innovation and product design, while leveraging the specialized expertise of manufacturers for wafer fabrication, packaging, and testing. By collaborating with renowned production partners, we ensure that our DRAM chips meet the standards of quality, reliability, and performance of our customers. Our main fabrication partner, PSMC, a Taiwan-based company, is one of the largest dedicated DRAM foundries globally with which we have established long-term strategic partnership. PSMC handles the intricate process of wafer fabrication, which involves transforming raw materials into high-performance semiconductor wafers. Following fabrication, the wafers are delivered to our DRAM packaging and testing service providers, where they undergo assembly, rigorous testing, and quality assurance processes to ensure they meet our specifications.

The fabless model offers significant strategic advantages, particularly in terms of cost efficiency and risk mitigation. By partnering with established foundries like PSMC and DRAM module manufacturers like ADATA, we avoid the substantial capital expenditures and operational complexities associated with owning and maintaining fabrication, packaging, and testing facilities. Additionally, our partners are responsible for procuring the majority of the raw materials required for production, further reducing our operational burden. This model also allows us to benefit from the advanced technologies and economies of scale that our partners bring to the table, ensuring that our DRAM products remain competitive in a rapidly evolving market.

The production timeline under this model is highly efficient. The fabrication of wafers typically takes four to five months, after which the wafers are transported to OSAT companies such as FATC and ChipMOS for packaging and testing. This phase generally requires approximately 10 to 14 days, depending on the complexity and volume of the order. Throughout the entire process, we maintain close collaboration with our partners to monitor quality, address any technical challenges, and ensure timely delivery. By adopting the fabless model, we are able to deliver cutting-edge DRAM solutions to our customers while maintaining flexibility, scalability, and a strong focus on innovation.

Arrangements with Our Production Partners

Selection of Production Partners

We carefully select our production partners, and we evaluate them based on a range of factors, including technological expertise, degree of cooperation, product quality and quality control effectiveness, cost reliability, ability to meet our delivery timeline and production capacity.

According to Frost & Sullivan, it is a common practice among leading DRAM chip design companies, particularly in China, to work exclusively with one single or a limited number of suppliers for fabrication to ensure stable supply of production capacity and continual iterations of production technologies in line with the product iterations. Fabrication of our DRAM chip products require advanced technologies and there are only few foundries capable of providing DRAM fabrication services globally. The substantial capital investment required to build and operate such foundries also contributes to their scarcity. We currently work with PSMC as our main fabrication foundry supplier to ensure sufficient supply of quality chips. Our longstanding partnership with PSMC is fortified by mutual trust and understanding. In instances where production capacities may waver, PSMC demonstrates firm dedication by prioritizing our orders. As of December 31, 2025, PIHC held (i) approximately 99.97% partnership interests of Hangzhou Chuyuan, one of our Shareholders (which is expected to hold approximately [**REDACTED**]% shareholding of our Company upon the [**REDACTED**]), and (ii) approximately 19.82% of PSMC.

In addition, we have established cooperation with globally leading DRAM module manufacturers including ADATA and Ramaxel. We also maintain collaborative relationships with leading OSAT companies, including FATC and ChipMOS for packaging and testing services.

Wafer Fabrication

We work with PSMC to produce DRAM wafers. In our typical cooperation scenario, we and PSMC first enter into a non-disclosure agreement to maintain intellectual property rights. We then provide PSMC with basic preliminary information about our chip design, and work with them to finalize the layout. Once our design is taped out, PSMC fabricates a prototype for us to confirm. Once confirmed, PSMC procures necessary materials and mass production of the wafers can then be conducted, and we place actual purchase orders according to our business needs. As it takes an average of approximately four to five months from the time we place our orders to the delivery of the wafers, we work with PSMC to formulate semi-annual purchase plans.

During the Track Record Period, we entered into a framework agreement with PSMC and then placed monthly orders under the agreement to procure wafers. The salient terms of our framework agreements and orders with PSMC are set out below:

- *Duration*: The duration of the framework agreements with PSMC is one year, subject to automatic renewal unless either party provides a two-month notice of termination prior to the end of the contract term.

- *Minimum purchase requirement*: There is no minimum purchase requirement under the agreements with PSMC.

- *Pricing*: We negotiate the price for each order with PSMC, with reference to prevailing market rates.

- *Payment and credit term*: PSMC generally grants us a credit term of one month from the date of billing.

- *Warranty and product return*: PSMC provides a one-year warranty period for the products delivered to us. During the warranty period, we may return defective products. PSMC shall address the issue with us within five days, with compensation capped at the purchase price. If the product is discontinued, we are entitled to return the product. PSMC shall cover the costs for defects attributable to them, while we cover the costs for defects not attributable to PSMC.

- *Logistics*: Wafers shall be delivered to the locations designated by us under 2001 INCOTEMS Delivered Duty Unpaid (DDU).

- *Transfer of risks*: Risks are transferred from PSMC to us once the wafers are delivered to the locations designated by us.

- *Non-Disclosure*: Unless with our prior written consent from the other party and subject to certain exceptions, each party shall not disclose to any third parties or use or cause to be used by any third parties any confidential information obtained as a result of the framework agreement. The obligation of non-disclosure remains effective for 10 years irrespective of the term of the framework agreement.

- *Termination*: Both parties are entitled to terminate the agreement with 60 days' prior written notice.

Our Relationship with PSMC

We relied on PSMC, our main foundry partner, for the production of DRAM wafers during the Track Record Period. As a result, PSMC consistently ranked among our top five suppliers in each period during the Track Record Period, accounting for 49.1%, 42.4% and 26.1% of our total procurement in the respective periods, while procurement from our top five suppliers in each period during the Track Record Period accounted for 88.6%, 76.2% and 64.0%, respectively, of our total procurement for the respective periods. Our procurement from PSMC as a percentage of the total cost of sales decreased significantly during the Track Record Period mainly due to our increased procurement of DRAM chips used in our growing DRAM module business, which was further attributable to our decision to expand into and develop IT application innovation business. The cost of sales attributable to PSMC (including the cost of sales attributable to the purchase from PSMC through AP Memory) during the Track Record Period amounted to RMB336.4 million, RMB258.3 million and RMB282.8 million, accounting for 63.5%, 46.0% and 25.8% of our total cost of sales in the respective periods. During the Track Record Period, the procurement volume from PSMC (including the procurement attributable to the purchase from PSMC through AP Memory) amounted to 24.5 million GB, 21.1 million GB and 28.3 million GB for the respective period and the average procurement cost attributable to PSMC (including the procurement attributable to the purchase from PSMC through AP Memory) amounted to RMB10.7, RMB11.9 and RMB10.0 per GB, respectively. Our procurement volume from PSMC (including the procurement attributable to the purchase from PSMC through AP Memory) decreased from 24.5 million GB in 2023 to 21.1 million GB in 2024 mainly because we tightened inventory management in response to the volatile market condition.

In the typical collaboration model between fabless companies and foundries, a single foundry is usually responsible for the entire wafer fabrication and associated foundry services. According to Frost & Sullivan, there are only a limited number of foundries worldwide, which are currently capable of providing comprehensive DRAM wafer fabrication and foundry services.

As our main foundry supplier during the Track Record Period, PSMC was responsible for the performance of the majority of wafer fabrication and associated foundry services. The wafer fabrication and associated foundry services provided by PSMC include wafer loading, oxidation, pattern generation, photo resist (PR) coating, lithography exposure, PR development, thin film pattern etching, PR stripping and wafer acceptance testing.

Given the highly competitive and rapidly evolving nature of the DRAM market, where supply and demand dynamics can significantly impact pricing and availability, securing dedicated production capacity ensures a stable supply chain, which is essential to our business. Since PSMC was our main wafer foundry supplier during the Track Record Period and we have a long-standing partnership, we entered into a production capacity reservation agreement (the "**Production Capacity Reservation Agreement**") with PSMC in October 2021 which was primarily driven by the industry-wide tight production capacity at the relevant time to ensure supply chain certainty. Pursuant to the Production Capacity Reservation Agreement, PSMC committed to supplying and we committed to purchasing certain number of wafers according to an agreed schedule. The Production Capacity Reservation Agreement expired on December 31, 2024 after renewal on December 31, 2023. The DRAM market has then shifted into a phase of relatively balanced or surplus capacity, allowing industry participants more flexibility in planning and allocating resources. We believed maintaining operational agility through normal procurement arrangements better serves our business strategies than making rigid purchase commitments with PSMC. Therefore, we did not extend the Production Capacity Reservation Agreement or enter into new agreement or arrangement with PSMC to that effect upon the expiration of the Production Capacity Reservation Agreement.

Our Directors believe, and the Sole Sponsor concurs, that there is no material risk of terminating our business relationship with PSMC, taking into account the following key factors: (i) we have maintained a stable business relationship with PSMC for over 20 years (covering business relationship between PSMC's predecessor prior to its spun off from PIHC (formerly known as Powerchip Technology Corporation) and Zentel Japan since 2004); (ii) PIHC, a shareholder of PSMC, is also an indirect shareholder of our Group, further strengthening the business ties between both parties; (iii) we have been one of PSMC's long-term customers with predictable forecast, and our purchases accounted for 1.3%, 2.4% and 2.3% of the total revenue of PSMC for the three years ended December 31, 2024, respectively; (iv) there has been no past disruption in our business cooperations; (v) as a foundry, PSMC's core business depends on providing services to fabless companies, and terminating such relationship would negatively impact its revenue; (vi) an easing of capacity constraints in the DRAM industry may reduce competitive pressure on foundry service allocations; and (vii) we have established cooperation with PSMC that goes beyond purchase orders in our ordinary course of business, which involves joint development of advanced technologies such as 19nm and below nodes and certain 3D AI semiconductor solutions.

In addition, our Directors believes that our relationship with PSMC is mutually dependent, based on the following factors: (a) PSMC relied on our design capabilities to jointly develop DRAM products based on 19nm and below nodes because there are only a limited number of fabless companies that possess independent DRAM design capabilities at advanced process nodes, aside from leading international players; (b) PSMC has partnered with 10 supply chain partners, including us, to introduce certain 3D AI semiconductor solutions; (c) we maintain a stable and predictable order forecast; and (d) we have established a strong and long-term relationship with PSMC, which dates back to the period prior to our acquisition of Zentel Japan.

As wafers constitute our key raw materials and PSMC was our main third-party foundry supplier during the Track Record Period, we monitor potential alternative partners and maintain internal readiness to shorten the lead time for alternative foundry when necessary. As of the Latest Practicable Date, we had entered into a wafer fabrication agreement with an alternative foundry. Our Directors believe that we will be able to find alternative wafer foundry supplier in the event of relationship termination or supply chain disruption in relation to our current foundry suppliers, and that our existing design processes are adaptable to other foundry platforms with reasonable engineering effort and lead time.

Packaging and Testing

After the wafers are manufactured, they are shipped to an OSAT company for packaging into chips, which are then tested to ensure that they meet all the quality control procedures.

Specifically, packaging involves enclosing the DRAM chips in protective materials to ensure durability, thermal performance, and electrical connectivity. Advanced packaging techniques, such as flip-chip or TSVs, may be employed depending on the product requirements. Once packaged, the chips undergo rigorous testing to verify functionality, performance, and reliability. This includes electrical testing, speed grading, and stress testing under various environmental conditions. Defective units are identified and discarded, while passing units are prepared for shipment. Packaging and testing are critical steps to ensure that the final product meets both technical specifications and customer expectations, delivering high-quality, reliable memory solutions to the market. We also maintain collaborative relationships with leading OSAT companies, including FATC and ChipMOS for packaging and testing services. We provide order forecasts three months in advance on a monthly basis to OSAT companies for them to purchase the necessary materials. It usually takes our packaging and testing suppliers about 10 to 14 days for testing and packaging.

During the Track Record Period, we entered into framework agreements with OSAT companies and then placed orders under the framework agreement to procure testing and packaging services. The typical salient terms of our framework agreements and orders with major OSAT companies include: (i) the duration of the framework agreement is typically one year, subject to

automatic renewal unless either party provides a two-month notice of termination prior to the end of the contract term; (ii) the price for each order is negotiated with reference to prevailing market rates; (iii) we typically settle payments on a monthly basis and we are required to pay within 60 days upon receipt of invoices; and (iv) both parties are entitled to terminate the agreement with 60 days' prior written notice.

LOGISTICS AND INVENTORY MANAGEMENT

Logistics

We engage third-party logistics service providers for the delivery of finished goods to locations specified by our customers. We set strict standards for the transportation of our products that these third-party logistics service providers are required to follow and we evaluate the third-party logistics service providers periodically on their compliance and performance to ensure smooth delivery of products to customers. During the Track Record Period, we primarily engage logistics service providers in Taiwan and Hong Kong for delivery of products to our direct customers and distributors located in Taiwan, Hong Kong and mainland China.

Inventory Management

We attach great importance to our inventory health, assigning dedicated staff to provide management with regular reports on the status of inventory. We take inventory level into consideration when formulating procurement plans.

Our inventories mainly include raw materials, work in progress and finished goods. We have various policies in place to ensure effective inventory management, such as (i) adopting the first-in, first-out method, (ii) maintaining a safety stock to compensate for any unexpected increase in demand or delay in supply, (iii) tracking and monitoring the flow of goods and inventory levels through our BI system to enhance inventory turnover rates, ensuring that inventories do not remain in our warehouses for too long, and (iv) conducting regular stocktaking to ensure the accuracy of inventory records. For the three years ended December 31, 2025, our inventory turnover days were 115, 97 and 89 days, respectively. For details, please see "Financial Information — Discussion of Certain Key Consolidated Statements of Financial Position Items — Inventories."

SALES AND MARKETING

We have established a robust brand reputation and significant industry influence through sustained, comprehensive, and in-depth collaborations with top-tier companies across diverse application areas. Our "Zentel" brand was inherited from Zentel Japan, which boasts over 20 years of history. By adopting tailored strategies for customers in different industries and dedicating substantial resources to business development in emerging applications, we have solidified our position as a trusted partner in the global market. Our customer-centric approach ensures that we not only meet but exceed the expectations of our customers, fostering long-term relationships and driving mutual growth.

Our comprehensive customer strategy spans the entire process from customer acquisition to product delivery, further enhancing our industry influence and reputation. We maintain close contact with our customers to gain a deep understanding of their needs and the competitive landscape. Leveraging our thorough understanding of international market dynamics and customer requirements, we are able to position our products strategically, engage in collaborative product development, promptly address technical issues during production, and provide exceptional after-sales services. This holistic approach has enabled us to build a loyal customer base and establish ourselves as a leader in the industry.

We take a customer-centric marketing approach to build and expand our business relationships. By collecting direct feedback from customers and partners, we gain valuable insights that drive our business and operational strategies forward. We formulate targeted marketing strategies and participate in a variety of marketing activities, including exhibitions, forums, to meet our business promotion needs and enhance our brand awareness. As we continue to expand both domestically and globally, we are committed to optimizing our sales and marketing network to ensure comprehensive geographic coverage across existing and new markets.

Sales Channels

We have an experienced and highly trained sales and marketing team, consisting of 26 personnel as of December 31, 2025, who proactively identify market opportunities and design sales strategies. Our products are sold through both direct sales and distribution. The table below sets out a breakdown of our revenue in both absolute amount and percentage of our total revenue by sales channel for the periods indicated:

	For the year ended December 31,					
	2023		2024		2025	
	RMB'000	*% of revenue (%)*	*RMB'000*	*% of revenue (%)*	*RMB'000*	*% of revenue (%)*
Distribution	402,923	69.4	421,430	65.2	642,135	58.1
Direct sales	177,423	30.6	224,971	34.8	462,754	41.9
Total	**580,346**	**100.0**	**646,401**	**100.0**	**1,104,889**	**100.0**

Geographical analysis

Throughout the Track Record Period, China (including Hong Kong and Taiwan) was our major market and we derived approximately 80.8%, 77.3% and 87.8% of our total revenue from the customers located in China (including Hong Kong and Taiwan) for each of the three years ended December 31, 2025. The table below sets out a breakdown of our revenue by reference to the principal business locations of our customers for the years indicated:

	For the year ended December 31,					
	2023		2024		2025	
	RMB'000	*% of revenue (%)*	*RMB'000*	*% of revenue (%)*	*RMB'000*	*% of revenue (%)*
China (including Hong Kong and Taiwan)	468,724	80.8	499,361	77.3	971,327	87.8
Other countries and regions in Asia[(1)]	93,975	16.2	106,689	16.5	94,618	8.6
Western Europe	17,545	3.0	39,969	6.1	37,090	3.4
Other countries and regions[(2)]	102	0.0	382	0.1	1,854	0.2
Total	**580,346**	**100.0**	**646,401**	**100.0**	**1,104,889**	**100.0**

Notes:

(1) Other countries and regions in Asia mainly include Japan and Singapore.

(2) Other countries and regions mainly include the United States and Isarel.

Direct Sales

As of December 31, 2023, 2024 and 2025, we had 20, 25 and 38 direct sales customers, respectively, many of whom were industry-leading enterprises with strict quality standards and long product validation cycles. For the three years ended December 31, 2025, revenue from direct sales amounted to RMB177.4 million, RMB225.0 million and RMB462.8 million, respectively, representing 30.6%, 34.8% and 41.9% of our total revenue for the respective periods.

We typically reach our direct sales customers through marketing activities such as exhibitions, forums. The adoption of direct sales enables us to precisely understand and respond to customer requirements, allowing us to offer tailored products and services that meet our customers' specific needs. We acquire direct sales customers by leveraging our strong brand reputation and significant industry influence, built through long-term, comprehensive collaborations with leading companies across various application sectors, complemented by targeted marketing activities.

We enter into sales agreements with our direct sales customers, which typically do not have a specified duration, and both parties are entitled to terminate the agreement with one month's prior written notice. We are generally responsible for delivering our products to locations designated by our direct sales customers. The risks transfer to direct sales customers normally after they confirm receipt of our products. We typically do not allow our direct sales customers to return products to us except for limited reasons, such as product design defects or quality issues.

Distribution

We primarily sell our products through a distributorship model, where our role in relation to the distributors is as a seller/buyer. This approach allows us to efficiently manage payment term risks, reduce cash flow pressures, and gain logistical support, while also enabling us to rapidly establish regional sales networks and enhance market penetration. By leveraging distributors, we can streamline administration and logistics, effectively serving a large and diverse base of end customers across industries such as consumer electronics, network communications, automotive electronics, power edge computing and industrial control systems. According to Frost & Sullivan, it is an industry practice to adopt the distributorship model.

As of December 31, 2023, 2024 and 2025, we had 33, 36, 37 and 51 distributors, respectively. During these years, revenue from distributors amounted to RMB402.9 million, RMB421.4 million and RMB642.1 million, representing 69.4%, 65.2% and 58.1% of our total revenue for the respective periods.

Selection and Management of Distributors

We select distributors based on a comprehensive set of criteria, including their performance, customer base, technical capabilities, financial condition, and alignment with our marketing needs. Distributors are not exclusively engaged to sell our products, and during the Track Record Period, we have had no material unresolved disputes or lawsuits with them. Distributors purchase products directly from us without any commission arrangement, maintaining their own inventories and on-selling to end customers.

To ensure effective management, distributors report end customer information to us, including sales data, project details and shipping addresses. This enables us to monitor actual sales, track logistics, and mitigate risks such as channel stuffing and cannibalization among distributors.

For certain key end customers, we engage with direct price negotiation with end customers by providing quotes, while distributors are responsible for delivery and post-sales services. This dual approach ensures competitive pricing and high-quality customer support. Additionally, we conduct comprehensive evaluations of our distributors, and if a distributor underperforms or fails to meet our expectations, we terminate the cooperation.

We manage distributors similarly to our in-house sales team, setting annual sales targets and monitoring performance monthly. We provide distributors with recommended price ranges and support their sales and marketing efforts through training, technical assistance, and promotional activities. Distributors are required to adhere strictly to our stipulated price ranges when quoting end customers. This ensures consistency in pricing and protects our brand reputation.

We generally do not allow product returns except in cases of quality issues. Similarly, we are not contractually obliged to buy back the products from distributors even under exceptional circumstances, such as bankruptcy, liquidation, or termination of the agreements with them. This policy helps maintain inventory discipline and reduces financial risks. During the Track Record Period, we had not repurchased any products from our distributors under circumstances including the distributors' bankruptcy or liquidation, or termination of distributorship agreement.

During the Track Record Period, to the best of our knowledge, all of our distributors are Independent Third Parties who were not controlled by our former or current employees, did not use our brand or name nor receive any material advance or financial assistance from us.

Risk Management and Ethical Practices

We maintain strict internal policies to manage risks associated with distributorship, including regular monitoring of shipments, inventory levels, and end customer feedback. Distributors report to us on product shipment to their customers, allowing us to track product usage and adjust supply to prevent overstocking or channel stuffing.

To ensure ethical business conduct, we conduct evaluations of distributors on a regular basis, assessing criteria such as compliance with anti-corruption policies. We incorporate anti-commercial bribery clauses in our agreements with distributors and provide comprehensive training to employees on our ethical standards. Any violations, such as kickbacks or bribery, result in punitive measures or termination of the distributorship.

Salient terms

We enter into framework agreements and/or place purchase orders with distributor customers to procure our products. The salient terms of our standard agreements with distributors during the Track Record Period are set forth below:

- *Duration*. Our agreements with distributors typically do not have a specified duration.
- *Minimum purchase requirement*. There is no minimum purchase requirement or minimum sales target.
- *Pricing*. We provide a price range for our distributors' reference, and the price range is subject to market conditions. There is no term mandating selling prices to end-customers.
- *Payment and credit terms*. Payment terms granted to our distributors vary, ranging from full prepayment to 45-day credit period.
- *Sub-distribution*. Distributors are not restricted from appointing sub-distributors. During the Track Record Period, to the best knowledge, information and belief of our Directors, there were no sub-distributors engaged by our distributors.
- *Warranty*. We generally provide an one-year warranty period for the products delivered to our distributors. We are responsible for fixing quality issues or the replacement of our products during the warranty period.

- *Product returns*. During the warranty period, we will accept requests for product returns or exchanges from our distributors only if the products do not meet quality standards. Our product return policy is in line with industry practice, according to Frost & Sullivan.

- *Geographical exclusivity*. Distributors are authorized to sell our products within a designated region.

- *Non-Disclosure.* Unless with our prior written consent, distributors shall not disclose to any third parties any confidential information obtained as a result of the agreements with us. In case of breach, distributors shall compensate our loss including payment of liquidated damages. The obligation of non-disclosure remains effective irrespective of the term of our agreements with distributors and until the relevant confidential information becomes publicly available.

- *Termination*. Parties may not terminate the agreements with distributors and/or the relevant orders without justification. If our distributors cause early termination, they must compensate us for all losses and pay liquidated damages. Additionally, if payments are delayed beyond 10 days, we will be entitled to terminate the agreement and deduct any liquidated damages from the distributors' payable amounts.

Movement by geographic region

The below table sets forth the movement of our distributors by geographic region during the Track Record Period.

	For the year ended December 31,		
	2023	**2024**	**2025**
Number of distributors at the beginning of the period			
– PRC	1	5	7
– Overseas	32	31	30
Number of new distributors for the period			
– PRC	4	3	4
– Overseas	5	1	12
Number of distributors which ceased business relationship for the period			
– PRC	0	1	0
– Overseas	6	2	2
Net increase (or decrease) in number of distributors for the period			
– PRC	4	2	4
– Overseas	(1)	(1)	10
Number of distributors at the end of the period			
– PRC	5	7	11
– Overseas	31	30	40
Total	**36**	**37**	**51**

During the Track Record Period, we strengthened our distributor network to facilitate the sales of our products as our business expanded. In 2023, 2024 and 2025, we engaged nine, four and 16 new distributors, respectively. We stringently review our business relationship with distributors through periodic assessment. In 2023, 2024 and 2025, we terminated business relationship with six, three and two distributors, respectively, for reasons including (a) unsatisfactory sales performance or cooperation that did not meet our evaluation criteria, (b) changes in the distributors' business operations, and (c) replacement by other distributors designated by end customers or their affiliated entities.

OUR CUSTOMERS

The industries which our customers operate in include consumer electronics, network communications, automotive electronics, energy and industrial control equipment. For instance, we are a major DRAM chip supplier to a global leader in computer and printer manufacturing, a leading communication equipment manufacturer in Europe, a leading router manufacturer in China, and a prominent IoT SoC chip design company in China, solidifying our market leadership. These collaborations have not only solidified our market leadership but also provided us with invaluable feedback to continuously optimize our products and services. Leveraging the trust of our customers, we have achieved a leading market share in niche DRAM market, with our DDR3 products capturing considerable market share in the Chinese telecommunication operator market for WiFi6 & GPON, according to Frost & Sullivan. We have also made significant breakthroughs in the computer system market, particularly in the server projects of one of the world's largest mobile communication operators, where we established business relationships with several leading Chinese communication equipment manufacturers.

Currently, we are focused on the R&D, and market expansion of AI-driven memory products designed for storage and computing applications. We have also established strategic partnerships with leading AI computing power chip companies in China. As our AI-driven memory products continue to mature, we anticipate the emergence of more commercialized application scenarios in the AI field, further solidifying our role as a key player in the DRAM chip market.

Given the long product lifecycle and the high demand for product stability, we work closely with our customers during the R&D and design phases to ensure seamless technical integration. In the DRAM chip industry, the technical complexity of DRAM design, which must balance factors such as storage density, speed, power consumption and stability, creates significant technological barriers, according to Frost & Sullivan. As a result, there are relatively few companies globally that specialize in DRAM design, making it a highly specialized and competitive field, and leading customers have stringent qualification and certification requirements. Our deep technical expertise allows us to systematically assist customers in design and product development, while our top-tier service team supports customers in product anti-interference system validation and reliability reporting. With our strong technical capabilities and excellent service, we can accurately identify customer needs from the outset, deeply penetrate target markets, and collaborate with leading customers to develop high-quality products that meet their specific requirements.

Customer service lies at the core of our competitive edge. We offer professional technical support and consulting services to ensure our customers achieve the best possible experience throughout the product lifecycle, thereby enhancing customer loyalty. Leveraging our exceptional service experience we provide to our existing customers, we have successfully secured partnerships with renowned domestic and international customers. These collaborations have facilitated the application of our products and technologies across various scenarios, including smart TVs, audio-visual playback, computers, and servers.

Major Customers

Revenue generated from our top five customers in each period during the three years ended December 31, 2025 amounted to approximately RMB387.6 million, RMB336.1 million and RMB479.2 million, representing approximately 66.8%, 52.0% and 43.4% of our total revenue for the respective periods. Revenue generated from our largest customer in each period during the three years ended December 31, 2025 amounted to RMB174.0 million, RMB87.5 million and RMB170.3 million, representing approximately 30.0%, 13.5% and 15.4% of our total revenue for the respective years.

The following table set forth our top five customers for the respective periods indicated:

For the year ended December 31, 2023

Ranking	Customer	Principal business location	Product sold or service rendered	Downstream application by end customers[Note 10]	Method of procurement	Method of payment	Credit term	Transaction amount	% of total revenue of the Group	Year of commencement of business relationship with our Group[Note 1]
								RMB'000	%	
1. . . .	CHONG WAI (HONGKONG) ELECTRONICS LIMITED (創威(香港)電子有限公司)) ("**CHONG WAI**")[Note 2]	Hong Kong	DRAM chips	Various applications including router, printer and smart home appliances	Distribution	Wire transfer	45 days	174,016	30.0	2020
2. . . .	Customer Group A[Note 3]	China	DRAM chips	Router	Direct sales	Wire transfer	30 days	101,790	17.5	2021
3. . . .	HONGKONG NBW ELECTRONIC CO., LTD (香港新光維電子有限公司) ("**NBW ELECTRONIC**")[Note 6]	Hong Kong	DRAM chips and KGD wafers	Camera	Distribution	Wire transfer	30 days	39,066	6.7	2022
4. . . .	Customer B[Note 4]	Japan	DRAM chips	Printer, hard disk drive (HDD), automotive electronics	Distribution	Wire transfer	Monthly 10 days	36,694	6.3	2019
5. . . .	BLUE OCEAN Group[Note 7]	Hong Kong	DRAM chips and modules	Various applications including industrial control, PCs, servers and network security	Distribution	Wire transfer	Full prepayment	36,066	6.3	2023
Total .								**387,632**	**66.8**	

For the year ended December 31, 2024

Ranking	Customer	Principal business location	Product sold or service rendered	Downstream application by end customers[Note 10]	Method of procurement	Method of payment	Credit term	Transaction amount	% of total revenue of the Group	Year of commencement of business relationship with our Group[Note 1]
								RMB'000	%	
1. . . .	BLUE OCEAN Group[Note 7]	Hong Kong	DRAM chips, modules and KGD wafers	Various applications including industrial control, PCs and servers	Distribution	Wire transfer	Full prepayment	87,513	13.5	2023
2. . . .	CHONG WAI[Note 2]	Hong Kong	DRAM chips	Various applications including router, printer and smart home appliances	Distribution	Wire transfer	30 days	77,409	12.0	2020
3. . . .	Customer Group A[Note 3]	China	DRAM chips	Router	Direct sales	Wire transfer	30 days	68,644	10.6	2021
4. . . .	Customer C[Note 5]	Singapore	DRAM chips	Printer	Direct sales	Wire transfer	Monthly 75 days	51,904	8.0	2011
5. . . .	NBW ELECTRONIC[Note 6]	Hong Kong	DRAM chips and KGD wafers	Camera	Distribution	Wire transfer	30 days	50,642	7.9	2022
Total . .								**336,112**	**52.0**	

For the year ended December 31, 2025

Ranking	Name	Principal business location	Product sold or service rendered	Downstream application by end customers[Note 10]	Payment Method	Method of procurement	Credit Term	Transaction amount	% of total revenue of the Group	Year of commencement of business relationship with our Group
1 . . .	CHONG WAI[Note 2]	Hong Kong	DRAM chips, modules	Various applications including router, printer and smart home appliances	Wire transfer	Distribution	15 days	170,293	15.4	2020
2 . . .	Customer Group D[Note 8]	China	DRAM modules	Various applications including industrial PCs and enterprise-level servers	Wire transfer	Direct Sales	60 days	105,828	9.6	2023
3 . . .	Customer Group A[Note 3]	China	DRAM chips	Router	Wire transfer	Direct Sales	30 days	78,356	7.1	2021
4 . . .	BLUE OCEAN Group[Note 7]	Hong Kong	DRAM chips, modules and KGD wafers	Various applications including industrial control, PCs and servers	Wire transfer	Distribution	Full prepayment	63,786	5.8	2023
5 . . .	Customer E	China	DRAM modules	Server	Wire transfer	Direct Sales	90 days	60,970	5.5	2025
Total .								**479,233**	**43.4**	

Notes:

(1) Where applicable, the year of commencement of business relationship with our Group refers to when the relevant customer first began its business relationship with Zentel Japan, our major subsidiary. See "History, Development and Corporate Structure — Zentel Japan" for details.

(2) CHONG WAI, a private company incorporated in 2010 with paid-up capital of HKD46,650,000, is principally engaged in the trading of electronic components, whose downstream customers are mainly leading PRC companies in the network communication and smart home appliances industries whose annual revenues during the Track Record Period typically exceeded RMB1.0 billion. Sales to CHONG WAI decreased from RMB174.0 million in 2023 to RMB77.4 million in 2024. The growth in 2023 was supported by our strategic measures following the 2022 market downturn, mainly attributable to (i) the temporary shortfall in upstream supply in 2024 amid a rebound in DRAM market demand following the contraction in 2023, and (ii) the impact of increased availability of lower-priced alternative components in 2024 following adjustments in end customers' purchase standards. Sales to CHONG WAI increased to RMB170.3 million in 2025, mainly attributable to the increase in the average selling price and sales volume to CHONG WAI, which was further attributable to the upward cycle in the DRAM industry in 2025.

(3) Customer Group A, a group of companies incorporated in 2000, 2008 and 2021, respectively, are principally engaged in the manufacturing and sales of network communication equipment. The paid-up capital of entities in Customer Group A is RMB500.0 million, RMB200.0 million, RMB20.0 million and RMB50.0 thousand, respectively.

(4) Customer B, a joint stock company incorporated in 1961 with paid-up capital of JPY13,672,000,000, is principally engaged in trading of electronics, whose major downstream customer are Japanese conglomerates whose annual revenues during the Track Period Record typically exceeded JPY500.0 billion.

(5) Customer C, a private company incorporated in 1970 with issued and paid-up capital of SGD5,328,737,000, is principally engaged in manufacturing of printers, manufacturing and repair of electronic office machinery and equipment, and manufacturing and repair of engineering and scientific instruments.

(6) NBW ELECTRONIC, a private company incorporated in 2018 with paid-up capital of HKD10,000, is principally engaged in sales of electronic products and trading of electronic components, whose downstream customers are mainly leading PRC companies in the semiconductor industry whose annual revenues during the Track Record Period typically exceeded RMB500.0 million.

(7) BLUE OCEAN Group comprises (a) SHENZHEN LANHAI CHENXI ELECTRONIC TECHNOLOGY CO. LIMITED* (深圳嵐海晨曦電子科技有限公司) incorporated in 2019 with registered capital of RMB10.0 million and (b) BLUE OCEAN (HONG KONG) ELECTRONIC TECHNOLOGY CO., LIMITED (香港藍海晨曦電子科技有限公司) incorporated in 2021 with paid-up capital of HKD10,000. BLUE OCEAN Group is principally engaged in manufacturing and sales of computer hardware and software, instruments and meters, and IC products and components, whose downstream customers are mainly PRC public and private entities in the IT application innovation industry.

(8) Customer Group D, a group of companies incorporated in 1997 and 2020, respectively, are principally engaged in industrial control computer and system manufacturing. The paid-up capital of entities in Customer Group D is approximately RMB3,225.8 million and RMB602.0 million, respectively.

(9) Customer E, a private company incorporated in 2014 with paid-up capital of RMB1,431,330,000, is principally engaged in the manufacturing and sales of electronic, IT, energy, smart home and monitoring equipment.

(10) The downstream application by end customers is determined based on our best knowledge taking into account our understanding of the profiles of our customers, for example, their principal business activities as publicly available, and our communications with them during our daily business operations.

During the Track Record Period, sales volume of our DRAM modules consistently increased during the Track Record Period due to our decision to expand into and develop DRAM modules business. Our DRAM modules primarily address the mainstream market and are widely used in high-end intelligent products, such as industrial high-performance PCs, data centers and enterprise-level servers, which are key products in the IT application innovation industry. The growing demand from the downstream customers of our DRAM modules was attributable to a combination of favourable market dynamics and favourable government policies. According to Frost & Sullivan, demand for DRAM modules grew rapidly in response to accelerated digitalization, expansion of data centres, artificial intelligence and IoT applications. These industry-wide developments substantially drove the need for reliable and cost-efficient DRAM modules, providing a strong demand base for the Group's products. In addition, according to Frost & Sullivan, the development of IT application innovation industry is aimed at addressing long-term overseas supply chain dependencies by establishing China's own IT foundation, encompassing domestic alternatives for

CPUs storage and database services, etc. Benefiting from the technological rise of local manufacturers and the promotion of the Internet of Things and domestic substitution policies, demand for domestically produced DRAM modules has grown steadily.

Against this industry backdrop, demand for DRAM modules expanded rapidly, directly driving our sales growth. Leveraging the strong market demand, the revenue contribution from our DRAM modules business increased from 8.1% in 2023 to 21.3% in 2024, and further to 38.8% in 2025. This growth was accompanied by a shift in our customer mix. Our sales to BLUE OCEAN Group, a customer of our DRAM modules, was RMB36.1 million in 2023, RMB87.5 million in 2024 and RMB63.8 million in 2025. It was our fifth, largest and fourth largest customer in 2023, 2024 and 2025, respectively. We established our business relationship with BLUE OCEAN Group in 2023 as part of our strategic initiative to expand our DRAM module business by engaging new distributors with sales capabilities in this business segment. The major downstream applications of the DRAM modules we sold through BLUE OCEAN Group include consumer electronics, servers, and desktop computers, enabling us to strengthen penetration into mainstream downstream applications and capture the industry's structural shift toward DRAM module demand.

During the Track Record Period, to the best knowledge of our Directors, none of our Directors, their associates or any of our current Shareholders (who, to the knowledge of our Directors, own more than 5% of our share capital) had any interest in our five largest customers in any period during the Track Record Period that are required to be disclosed under the Listing Rules.

Pricing

We price our products based on a variety of factors, including: (i) the costs of relevant products, which encompass production, R&D expenses and operational costs, and may vary depending on the type of products, (ii) customer demand, and (iii) the competitive landscape, which takes into account our strengths and weaknesses relative to our competitors, their pricing strategies and our customers' cost sensitivity. In addition, we adopt different pricing strategies across different product lines. Once we set the base prices according to these factors, we adjust the pricing on a case-by-case basis in consideration of specific requirements of our customers.

OUR SUPPLIERS

Our major suppliers are (i) our production partners including (a) wafer fabrication service provider and (b) packaging and testing service providers, as well as (ii) the suppliers of other raw materials. Our key raw materials during the Track Record Period are wafers. For details of our arrangement with our production partners and suppliers, please see "Production and Procurement" in this section. The purchases from our top five suppliers in each period during the three years ended December 31, 2025 amounted to approximately RMB475.9 million, RMB451.1 million and RMB754.2 million, representing approximately 88.6%, 76.2% and 68.7% of our total purchase amount for the respective periods. The purchase from our largest supplier amounted to RMB263.6 million, RMB250.7 million and RMB282.8 million, representing approximately 49.1%, 42.4% and 25.8% of our total purchase amount for the respective periods.

During the Track Record Period, to the best knowledge of our Directors, none of our Directors, their associates or any of our current Shareholders (who, to the knowledge of our Directors, own more than 5% of our share capital) had any interest in our five largest suppliers (except for PSMC) in any period during the Track Record Period that are required to be disclosed under the Listing Rules.

The following table set forth our top five suppliers for the respective periods indicated:

For the year ended December 31, 2023

Ranking	Supplier	Principal business location	Product purchased or service rendered	Method of payment	Credit term	Purchase amount	% of total purchase amount of the Group	Year of commencement of business relationship with our Group[Note 1]
						RMB'000	*%*	
1.	PSMC[Note 2]	Taiwan	DRAM wafers (including foundry services)	Wire transfer	Monthly 30 days	263,627	49.1	2004
2.	Ufct Technology Co., Limited (聯合創泰科技有限公司) ("**Ufct**")[Note 5]	Hong Kong	DRAM products	Wire transfer	45 days	70,451	13.1	2023
3.	FATC[Note 3]	Taiwan	IC packaging and testing services	Wire transfer	Monthly 60 days	67,113	12.5	2007
4.	ChipMOS[Note 4]	Taiwan	IC packaging and testing services	Wire transfer	Monthly 60 days	56,585	10.5	2007
5.	Supplier A[Note 6]	Hong Kong	DRAM products	Wire transfer	Monthly 30 days	18,122	3.4	2023
Total . .						**475,898**	**88.6**	

For the year ended December 31, 2024

Ranking	Supplier	Principal business location	Product purchased or service rendered	Method of payment	Credit term	Purchase amount	% of total purchase amount of the Group	Year of commencement of business relationship with our Group[Note 1]
						RMB'000	*%*	
1.	PSMC[Note 2]	Taiwan	DRAM wafers (including foundry services)	Wire transfer	Monthly 30 days	250,664	42.4	2004
2.	FATC[Note 3]	Taiwan	IC packaging and testing services	Wire transfer	Monthly 60 days	75,684	12.8	2007
3.	ADATA Group[Note 7]	Taiwan	DRAM module assembly services	Wire transfer	30 days	55,320	9.4	2023
4.	ChipMOS[Note 4]	Taiwan	IC packaging and testing services	Wire transfer	Monthly 60 days	38,328	6.5	2007
5.	Supplier A[Note 6]	Hong Kong	DRAM products	Wire transfer	Monthly 30 days	31,062	5.1	2023
Total . .						**451,058**	**76.2**	

For the year ended December 31, 2025

Ranking	Supplier	Principal business location	Product purchased or service rendered	Method of payment	Credit term	Purchase amount	% of total purchase amount of the Group	Year of commencement of business relationship with our Group
1	PSMC[Note 2]	Taiwan	DRAM wafers	Wire transfer	Monthly 30 days	282,831	25.8	2013
2	ADATA Group[Note 7]	Taiwan	DRAM module assembly services	Wire transfer	30 days	281,330	25.6	2023
3	FATC[Note 3]	Taiwan	IC packaging and testing services	Wire transfer	Monthly 60 days	72,801	6.6	2007
4	JIUBAN (HK) SEMICONDUCTOR LIMITED (久半(香港)半導體有限公司)[Note 8]	Hong Kong	DRAM products	Wire transfer	Full prepayment	61,672	5.6	2025
5	Supplier Group B[Note 9]	PRC	DRAM products	Wire transfer	Monthly 45 days	55,540	5.1	2023
Total . .						**754,174**	**68.7**	

Notes:

(1) Where applicable, the year of commencement of business relationship with our Group refers to when the relevant supplier first began its business relationship with Zentel Japan, our major subsidiary. See "History, Development and Corporate Structure — Zentel Japan" for details.

(2) PSMC, a company incorporated in 2008 with paid-up capital of TWD41,731,409,360 and listed on Taiwan Stock exchange with stock code 6770, is principally engaged in foundry services, sales, development, and manufacturing memory IC products including DRAM products. In 2004, PSMC's predecessor prior to its spun off from PIHC (formerly known as Powerchip Technology Corporation) commenced its business relationship with Zentel Japan.

(3) FATC, a company incorporated in 1990 with paid-up capital of TWD4,422,222,230 and listed on Taiwan Stock Exchange with stock code 8131, is principally engaged in packaging, testing, and module manufacturing services for memory IC products.

(4) ChipMOS, a company incorporated in 1997 with paid-up capital of TWD7,272,401,260 and listed on Taiwan Stock exchange with stock code 8150, is principally engaged in packaging, testing, and module manufacturing services for memory IC products and other IC products.

(5) Ufct, a private company incorporated in 2013 with paid-up capital of HKD5,000,000, is a wholly owned subsidiary of Supplier Group Company C, which in turn is a company listed on Shenzhen Stock Exchange. Ufct is principally engaged in the trading of electronic components and is a major distributor of SK Hynix in China. We began procuring DRAM products from Ufct in 2023 to support the growth of our DRAM module business, and purchases from Ufct became significant in the same year. The DRAM products supplied by Ufct during the Track Record Period were sourced from SK Hynix. We did not purchase directly from SK Hynix, as it primarily supplies products in the PRC through authorized distributors, which also offer credit terms, logistics and warehousing support.

(6) Supplier B, a private company incorporated in 2009 with paid-up capital of HKD1,000,000 and USD9,871,000, is principally engaged in trading of electronic components.

(7) ADATA Group comprises (a) ADATA incorporated in 2001 with paid-up capital of approximately TWD2,958.7 million and (b) ADVANCED DATA TECHNOLOGY (SUZHOU) CO., LTD (威方科技(蘇州)有限公司) incorporated in 2007 with paid-up capital of USD19.0 million. ADATA Group is principally engaged in manufacturing and sales of DRAM and other memory IC products.

(8) JIUBAN (HK) SEMICONDUCTOR LIMITED (久半(香港)半導體有限公司), a private company incorporated in 2025 with paid-up capital of HKD10,000, principally engaged in the manufacturing and sales of semiconductor products.

(9) Supplier Group C comprises Ufct, Supplier C and Supplier C1, all of which are subsidiaries of Supplier Group Company C. Supplier C, a private company incorporated in 2022 in Hong Kong with paid-up capital of HKD1.0 million, is principally engaged in trading of electronic components. Supplier C1, a limited liability company established in the PRC in 2023 with registered capital of RMB70 million, is principally engaged in the R&D, production and sales of enterprise level storage products. We began procuring DRAM products from Ufct in 2023 and began procuring DRAM products from Supplier C and Supplier C1 in 2025. The purchase amounts of our Group from Ufct, Supplier C and Supplier C1 are calculated on a consolidated basis since 2025.

Procurement of Raw Materials, Components and Parts

Wafers produced by PSMC accounted for the largest portion of our costs for raw materials during the Track Record Period. In addition to wafers, we procure DRAM chips, which are further integrated in our DRAM modules, and other electronic components and parts. We procure these raw materials, components and parts in accordance with our sales plans.

We generally do not enter into long-term supply agreements. Instead, we enter into purchase agreements and place purchase orders with our suppliers based on our purchase and production schedules. The typical salient terms of our standard purchase agreement and purchase orders with our major suppliers during the Track Record Period are set forth below:

- *Duration*. The supply agreements typically do not have a specified duration.
- *Minimum purchase requirement*. There is no minimum purchase requirement under the supply agreements.
- *Pricing*. Pricing terms with our suppliers mainly depend on the prevailing market rates but may also depend on the quantities that we purchase.

- *Payment and credit terms*. Payment terms granted by our suppliers vary depending on a number of factors, such as our relationships with them and the size of the transaction. For example, some suppliers require payment in advance, while some suppliers grant us a 30-day credit period after the products are accepted as qualified.

- *Warranty*. We are typically entitled to a warranty period of one year to three years. Our suppliers are responsible for fixing of the replacement of products during the warranty period.

- *Product returns*. During the warranty period, our suppliers are responsible for the return of products for quality reasons as requested.

- *Non-Disclosure*. Unless with our prior written consent, suppliers shall not disclose to any third parties any confidential information obtained as a result of the purchase orders. The obligation of non-disclosure remains effective irrespective of the terms of the purchase orders.

- *Termination*. If the products fail to meet specifications upon inspection, the supplier must replace them or provide a full refund, covering all associated costs. If the replaced products still do not conform, we have the right to terminate the purchase agreement, cancel the order, recover all payments, and claim liquidated damages.

Please see "Production and Procurement — Arrangements with Our Production Partners" in this section for the salient terms of the agreements with our production partners.

During the Track Record Period and up to the Latest Practicable Date, we did not experience any material breach of contracts on the part of our suppliers or delay in delivery of our orders from our suppliers, nor did we have any material disputes with our suppliers.

RESEARCH AND DEVELOPMENT

We are committed to innovation and focus on the R&D of our technology platform and products. Our technology platform undergoes continual iterations and refinement. We consistently dedicated ourselves to the development and design of high-bandwidth, low-power, and high-reliability memory solutions. With a comprehensive product portfolio that spans the full range of DRAM types, we offer a complete suite of memory solutions tailored for a wide array of applications, including consumer electronics and network communications such as set-top boxes, smart home appliances and IoT devices, as well as automotive electronics, energy and industrial control systems.

Notably, we have achieved significant breakthroughs in the field of high-reliability application. Our DRAM design with ECC technology provides a highly reliable memory solution for industrial control machinery and equipment operating in harsh environments. In addition, by leveraging TSV and hybrid bonding technologies, we have developed a multi-layer wafer-level stacked high-bandwidth memory solution, which has reduced power consumption by 50%, further solidifying our leading position in innovative memory solutions that offer high computing power with low energy consumption. Meanwhile, we are working closely with our wafer production partner to advance the design and development of DRAM products based on 19nm and below advanced nodes, ensuring future product competitiveness.

We invested significant resources into the R&D of our technology platform and products. In 2023, 2024 and 2025, we incurred research and development expenses of RMB77.2 million, RMB95.8 million and RMB102.1 million, representing 13.3%, 14.8% and 9.2% of our revenue during the respective periods.

Our R&D Team

We are supported by a robust R&D team comprising semiconductor industry veterans with profound expertise across the areas of DRAM Design. Our R&D team is jointly led by Mr. Kim Joonho, who was responsible for overseeing DRAM design and marketing at SK Hynix, Infineon Technologies, Jeju Semiconductor and Winbond Electronics before joining our Group in 2021, and Mr. Kubo Takashi, who currently oversees our R&D efforts in Japan, had extensive experience in the design and development of DRAM, flash memory, customized cache memory, and customized high-bandwidth memory at Mitsubishi Electric, Renesas Electronics and Zentel Japan.

As of December 31, 2025, our R&D team is comprised of 86 members, representing approximately 53.4% of our total employees. All of our R&D personnel hold a bachelor's degree or higher, with most specializing in electronic engineering. Our R&D department is primarily constituted by our R&D teams in Hangzhou and Japan. Our Hangzhou R&D team, which had 57 members as of December 31, 2025, focuses on the development of standardized DRAM chip products. The team is led by core experts from South Korea who have working experience on designing cutting-edge products such as DDR4, DDR5, LPDDR4, and LPDDR5 at major global brands. Our Japan R&D team, which comprised 10 members as of December 31, 2025 specializes in customized DRAM products and stacked structure products such as high-bandwidth memory. Our Japan team is led by Mr. Kubo Takshi, who has been working in Zentel Japan since its inception in 2003, as well as core experts with expertise in circuit design (including array, peripheral, interface, power generator, etc.), design software and tools and testing equipment.

Our teams in Hangzhou and Japan maintain a highly collaborative and synergistic working relationship, leveraging their respective expertise to drive innovation in advanced memory technologies. A prime example of this collaboration is our work on high-bandwidth memory, a cutting-edge solution that involves vertically stacking multiple DRAM chips to achieve superior performance. In this process, our Hangzhou R&D team takes the lead in optimizing chip performance by enhancing processing speed and reducing power consumption, ensuring the individual chips meet the highest standards of efficiency and reliability. Meanwhile, our Japan R&D team specializes in the intricate process of stacking these refined chips, utilizing their advanced technical capabilities to achieve precise integration and maximize overall performance. This seamless partnership not only accelerates the development cycle but also ensures that our high-bandwidth memory products deliver high quality and reliable performance, meeting the demands of next-generation computing and data-intensive applications.

Our R&D Mechanism

Through continuous accumulation of experience in iterative research and development, we have established a two-dimension design and R&D management system. This system features vertical collaboration between our R&D and business departments, as well as horizontal coordination among specialized R&D teams. This dynamic design mechanism enables us to effectively address the ever-evolving technical demands of the memory industry, significantly enhancing the predictability and efficiency of future development efforts.

Our design and R&D are carried out as a group effort in close collaboration between our different departments. Our sales and marketing department, who are deeply rooted in the industry and closer to customers, is responsible for the initial conceptualization of product candidates, which is typically derived from in-house ideas and information collected from customers. Our R&D department, comprising our Hangzhou team focusing on standardized product development and our Japan team focusing on high-bandwidth memory development, is responsible for the design and development of our products. Apart from our R&D department members, certain members of our sales and marketing department also possess technical backgrounds which we believe directly

contribute to an effective and seamless collaboration among the different departments for a successful and smooth product design. For details of our design process and the involvement of our various departments in the process, please see "Our Products and Solutions — Our Design Process" in this section.

Our R&D Achievements

We have consistently demonstrated our ability to innovate and iterate technology, driving advancements in product performance, customization, and R&D efficiency. Our comprehensive experience in technological iteration has provided us with a deep understanding of customers' diverse needs for memory solutions, allowing us to better meet their demands for customized products in terms of response speed and efficiency. Please see "Our Technologies" in this section for details of our key technologies in connection with our product offerings.

We have inherited the long-standing R&D experience of Zentel Japan, which was established in 2003, and core R&D experts, including Mr. Kubo Takashi. Building on our extensive experience and iterative approach in technology development from SDR to DDR4 products, we possess proprietary R&D capabilities in DRAM products and AI memory-computing solutions. According to Frost & Sullivan, we are one of the few domestic DRAM chip design company which possesses the complete iterations of DRAM products from SDR to DDR4. Leveraging our continuous R&D efforts in enhancing the design processes, we can enhance product yield and reduce costs in testing and other critical procedures in the manufacturing process. This commitment to technological advancement ensures that our DRAM products meet the stringent demands of high-reliability applications across diverse industries.

Below are key examples that highlight how our iterative technological advancements have led to significant breakthroughs in product design, customization, and development efficiency:

1. *Enhancing Product Performance through Design Improvements.* In respect of the standard 512Mb DDR2 product, which typically operates at 1.8V with a speed of 1,066Mbps, we introduced a 1.5V voltage design based on our deep understanding of the product technology, which not only reduced power consumption but also made the product compatible with variable (i.e. both 1.8V and 1.5V) power supplies. In addition, our revamped product achieved a speed of 1,333Mbps, significantly improving data transfer efficiency compared to the standard product. Furthermore, through design improvements, we increased the memory array from the standard 512 cells/BL to 688 cells/BL, resulting in a nearly 10% reduction in chip size compared to products from other companies using the same process technology.

2. *Meeting Customization Needs through Technical Adaptation.* Leveraging our expertise in DRAM chip technology, we have developed DRAM module products that are highly compatible with various CPUs from mainstream domestic manufacturers, providing a solid technical foundation for customized product development. For instance, in response to our customers' specific needs for higher reliability and additional value-added features, we successfully integrated our current technology (i.e. SECDED (single error correction, double error detection) ECC functionality) into an existing 25nm 4Gb DDR3 product. This adaptation was made possible by our iterative understanding of different products and functionalities, fulfilling specific customization requirements of our customers.

3. *Improving R&D Efficiency through Technological Accumulation.* During our product development process, we endeavor to shorten the development timeline from design to testing by maximizing the repeated utilization of existing design and programming resources, thereby reducing costs and improving efficiency. For example, during the development of a 25nm 2Gb DDR3 product, we leveraged our accumulated knowledge from similar products (for example, our 1Gb DDR3 product) to introduce a faster and more reliable circuit verification system. This innovation helps us shorten the overall product development cycle.

Our R&D Capabilities in AI Memory-Computing Solutions

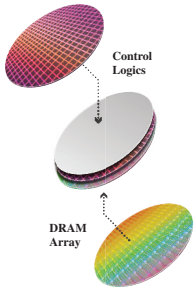
Leveraging our technical expertise across disciplines, we are developing key technologies relating to chip design, DRAM testing, and more importantly, AI memory-computing solutions which we believe will underscore our future competitiveness. High-bandwidth memory is an advanced memory technology designed to deliver significantly higher bandwidth compared to traditional DRAM solutions. It achieves this by stacking multiple DRAM chips vertically and connecting them using TSVs, which reduces data travel distance and increases speed. High-bandwidth memory is commonly used in high-performance applications such as GPUs, AI accelerators, and data centers, where large amounts of data need to be processed quickly. Unlike traditional DRAM modules, High-bandwidth memory is often integrated directly with processors or logic chips in a 2.5D or 3D configuration, enabling faster data transfer and lower power consumption. High-bandwidth memory products are poised to play a critical role in overcoming memory bottlenecks in future AI systems and are on track to become the mainstream memory solution for GPUs.

Our AI memory-computing solutions under development

Our AI memory-computing solutions are designed to address the storage bottlenecks in data-intensive AI applications, enhancing computational efficiency and enabling memory computing integration. Sets forth below are our key AI memory-computing solutions currently under development.

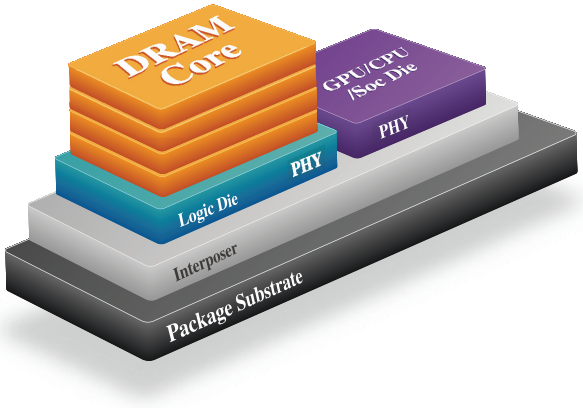
High-bandwidth 3D stacked DRAM chip. Our high-bandwidth 3D stacked DRAM chip utilizes heterogeneous integration technology, employing bumpless hybrid bonding to vertically interconnect the logic and DRAM layers. The ultra-fine bonding pitch not only significantly enhances performance but also reduces power consumption and latency. Significantly, the logic and DRAM wafers can be manufactured using distinct process technologies, enabling the creation of highly customized memory solutions that are optimized for achieving both high bandwidth and low power consumption.

Additionally, regarding multi-core processors, we are developing a solution where each logic core has its own dedicated memory core with direct access. This one-to-one design allows simultaneous access and enables high bandwidth (up to 57.6TB/s with 563 cores per layer in a 4-Hi stack). Each memory core has its own TSV interface, directly connecting to logic cores without redundant paths. This direct connection reduces energy consumption compared to 2.5D HBM solutions that require data to pass through an interposer. The following diagram depicts the design of our high-bandwidth 3D stacked DRAM chip.



The above features make our high-bandwidth 3D stacked DRAM chip a perfect fit for AI acceleration applications such as on-device AI inference for large language models. We plan to commercialize our high-bandwidth 3D stacked DRAM chip in 2026.

High-bandwidth memory-centric DRAM chip for AI applications. High-bandwidth memory-centric DRAM chips are now the main solution for memory bottlenecks in AI applications. Traditional solutions use TSV and micro-bump technologies to stack DRAM wafers with a logic control wafer, and connect to logic chips through CoWoS packaging. This design effectively caters to the high-speed data processing and bandwidth demands of AI workloads. For example, while the latest DDR5 offers about 5,600 Mbps data transfer rates and 50 GB/s bandwidth, leading *high-bandwidth memory-centric* solutions can exceed 9.6 Gbps data transfer rate and 1 TB/s bandwidth. Our high-bandwidth memory-centric DRAM chip, known as "Hybrid-stacked Memory (HSM)" not only inherits the proven strengths of traditional high-bandwidth memory-centric DRAM solutions but also achieves a significant advancement in multilayer stacking technology. By employing hybrid bonding for die stacking, it out performs existing solutions in terms of TSV pitch, thermal distribution, and overall performance. See "— Our Technologies relating to AI memory-computing solutions — 2. Customized 3D-IC Stacking Technology" in this section. The following diagram depicts the design of our HSM chip.



The above features make our high-bandwidth memory-centric DRAM chip a perfect fit for computing centers. We anticipate commercializing our HSM chips in 2026.

Silicon Interposer for Advanced Packaging. We also offer customized silicon interposer solutions featuring higher interconnect density, enhanced bandwidth performance, and lower power consumption compared to traditional substrate packaging techniques. These advanced features are achieved through the use of TSVs, embedded silicon capacitors, and RDLs. Serving as the connection between high-bandwidth memory and SoC, our silicon interposer enables electrical interconnection between heterogeneous dies, making it a key component in high-performance chiplet chips and CoWoS-based packaging solutions.

In May 2025, we have entered into a procurement contract with a Chinese AI-computing company, Enrigin, in respect of the purchase of silicon interposer from us, which signified the commercialization of our silicon interposer solutions. The total contract sum of such procurement contract is approximately RMB1.65 million excluding tax, including sales of interposer of approximately RMB0.54 million and non-recurring engineering fees of approximately RMB1.11 million, both exclusive of taxes. Pursuant to the payment terms of the procurement contract, Enrigin is required to provide formal written notice by email to us to initiate production and supply arrangements, and shall make full payment within 60 working days thereafter. In addition, to better support Enrigin under this procurement contract, we may provide packaging design and process engineering technical field support, for which we will charge a fixed monthly service fee starting from the date of contract execution, subject to orders from Enrigin. The pricing of our silicon interposer is determined on a per-unit basis, with the unit price subject to the agreed product specifications and testing requirements. The parties may review and adjust the unit price to reflect changes in raw material costs, production yields, or market conditions, subject to mutual written consent.

Overall, our AI memory-computing solutions currently under development include three distinct technologies, each designed to address different performance and integration needs. Our high-bandwidth 3D stacked DRAM chip vertically integrates logic and DRAM layers, offering extremely short signal transmission distances and high bandwidth, though with limited memory capacity. This design significantly enhances performance while reducing power consumption and latency, making it ideal for on-device AI inference for large language models. Meanwhile, our high-bandwidth memory-centric DRAM chip utilizes TSV and micro-bump technologies to stack DRAM wafers with a logic control wafer. While offering bandwidth that exceeds traditional DRAM solutions but less than our 3D stacked solution, these chips provide substantially greater memory capacity, optimized for computing center applications. Complementing these memory solutions, our customized silicon interposer serves as a key infrastructure in 2.5D stacking designs, enabling electrical interconnection between heterogeneous dies. Feature higher interconnect density, enhanced bandwidth performance, and lower power consumption, our customized silicon interposer is a key component in high-performance chiplet chips and CoWoS-based packaging solutions.

Our Technologies relating to AI memory-computing solutions

To enable the development of our key AI memory-computing solutions, we have established a core set of proprietary technologies that drive performance and integration advantages. Set forth below are the technologies we have developed which form the cornerstone of our AI memory-computing solutions.

Wafer-on-Wafer 3D Heterogeneous Integration Technology. Our Wafer-on-Wafer 3D heterogeneous integration technology enables direct bonding of logic and DRAM wafers in a vertically stacked configuration. This approach eliminates the need for interposers, significantly reducing latency and power consumption while maximizing bandwidth. The resulting design, comprising one logic wafer and one DRAM wafer, delivers 6GB of capacity and a bandwidth of up to 12TB/s, all while achieving ultra-low power efficiency of <1pJ/bit.

This technology is particularly well-suited for AI and high-performance computing applications, where rapid data access and energy efficiency are critical. By minimizing data movement between memory and processing units, our Wafer-on-Wafer integration enhances real-time inference and training performance, making it ideal for data centers, autonomous systems, and other latency-sensitive workloads.

Customized 3D-IC Stacking Technology. To address the growing demand for high-bandwidth memory in AI accelerators and GPUs, we have developed a customized 3D-IC stacking technology capable of four to eight stacked layers, offering configurable capacities ranging from 2GB to 4GB and a bandwidth of up to 400GB/s, which is comparable with JEDEC HBM2E standards.

A key differentiator of our approach compared with the traditional TSV and micro-bump based stacking is our bumpless hybrid bonding Wafer-on-Wafer stacking scheme, which effectively overcomes the thermal management challenges of traditional designs. Stacking memory is accompanied by a vast number of input/output interfaces, resulting in substantial total power consumption, which gives rise to thermal management challenges. To address this issue, efficient heat dissipation from the heat source to the heat sink is crucial. Our bumpless hybrid bonding Wafer-on-Wafer stacking scheme demonstrates outstanding heat diffusion performance. Without the presence of bumps, the heat conduction area is increased, and the use of extremely thin polished wafers significantly accelerates heat diffusion across multiple layers. With our customized 3D-IC stacking technology including the bumpless hybrid bonding Wafer-on-Wafer stacking scheme, we intend to achieve ~1.5pJ/bit, which is one-third of the power consumption of conventional 2.5D-stacked HBM2E solutions (typically 4—5pJ/bit).

Chiplet-Based SiP Technology. For mobile and edge AI applications, we employ chiplet-based SiP technology, which integrates multiple memory and logic chiplets into a compact, high-performance module. Our mobile-optimized solution features eight channels, each with a 512Mb density (1Gb per die), delivering a total bandwidth of 136GB/s at an efficient 2pJ/bit.

This design prioritizes small form factor and low power consumption, making it ideal for smartphones, IoT devices, and other battery-powered systems. The modular chiplet architecture also allows for customization, enabling tailoring of memory configurations for specific AI workloads, from on-device neural networks to real-time sensor processing.

Independent Logic Chip Design & Development Technology. Logic chips serve as critical components in high-bandwidth memory systems, directly determining end-product performance and future scalability. We are independently designing logic chips tailored for high-bandwidth memory applications, fully compliant with JEDEC HBM2 and HBM2E standards. Our logic chips will enable protocol command translation and serial-to-parallel data conversion, ensuring rapid and accurate data transmission.

To optimize power efficiency, we integrate Data Bus Inversion to reduce read/write power consumption, while Command/Address Parity and DQ Parity functions safeguard signal integrity. For testability, our chips will incorporate IEEE 1500-compliant boundary-scan circuits for connectivity validation. Built on advanced process nodes, our logic chips are expected to achieve 1.6GHz clock speeds and 3.2Gbps data rates, empowering high-bandwidth memory products with high speed, ultra-stability, and low-power operation.

Memory-Cell-Based Integrated Passive Device Technology. To deliver exceptional power supply stability, we have developed a proprietary memory-cell-based Integrated Passive Device ("**IPD**") technology designed . Benchmark testing demonstrates that our solution achieves a capacitance density of 515 nF/mm2 at voltages below 1.5V, representing a 30% improvement over comparable industry solutions. Notably, when operating at optimized low-voltage conditions (0.75V), such IPD technology can deliver effective capacitance values up to 2060 nF/mm2, substantially exceeding conventional alternatives.

Such IPD solutions are available in multiple integration formats to address diverse system requirements, including (i) discrete 2D components, with individual IPD devices for conventional circuit implementations; (ii) 2.5D interposer integration, with embedded passive networks for advanced packaging architectures; and (iii) 3D wafer-level solutions, with high-density integration with memory wafers for 3D system designs. This flexible implementation approach, combined with superior electrical performance, enables our IPD technology to meet the most demanding power delivery requirements and support a broad range of high-performance applications.

Our R&D Cooperation with Third Parties

We are actively engaged in cutting-edge industry research with our business partners and professional and academic institutions. During the Track Record Period, we collaborated with several external institutions in various research and development efforts, including the development of advanced wafer processes and 3D stacked and customized high-bandwidth memory.

We have entered into a development agreement with PSMC to govern our joint R&D efforts in relation to the design of DRAM products based on 19nm and below nodes (the "**Development Agreement**"), which is a testament of our R&D prowess and our close collaboration with our production partners. The 19nm 8Gb DDR4 DRAM chip (the "**19nm Product**") developed under the Development Agreement complies with JESD79-4D standards for all speed bins, IDD/IDDQ/IPP, and is used in the niche market. Compared with our existing products, the 19nm Product uses a more advanced process node, which yields more dies per wafer, reducing unit costs. According to the Development Agreement, all the intellectual property rights in and to all inventions developed in the course of the development shall be jointly owned by PSMC and us. PSMC will pay us a fixed

development cost in relation to the development of such products and we agree to engage PSMC exclusively for the foundry services. In terms of profit sharing, and PSMC will pay us certain percentage of the net sales of the products as royalties upon mass production, in consideration of the non-exclusive rights we grant to PSMC, among other things, to use, implement, remake and modify the technology in relation to the 19nm Product to manufacture, sell, offer for sale, import and/or distribute the 19nm Product. We reserve the rights to sell the 19nm Product by ourselves. We expect to commence mass production of the 19nm Product in the third quarter of 2027 and realize commercial sales of the 19nm Product in the fourth quarter of 2027.

The strategic partnership under the Development Agreement reflects our broader objective of enhancing our product competitiveness. PSMC, as a leading international foundry, brings cutting-edge production technologies and industry-leading manufacturing yields, laying a strong foundation for the development of advanced DRAM products. Importantly, the 19nm DRAM process represents the most advanced node currently available in China, offering clear advantages in both cost structure and performance, and is expected to significantly enrich our product portfolio. Furthermore, we expect to leverage the benefits of the 19nm and below nodes by incorporating them into our AI memory-computing solutions, including 3D stacked and HSM products, to support higher memory density and better fulfill evolving customer requirements.

From PSMC's standpoint, we believe that our collaboration also delivers substantial strategic value, which is reflected by its willingness to pay the development costs under the Development Agreement. By tapping into our robust DRAM design and architecture expertise, PSMC can shorten development cycles and reduce technical risks associated with advanced node products. The collaboration allows PSMC to accelerate its expansion into advanced DRAM nodes in a more cost-effective manner. Moreover, the exclusive production arrangement ensures a stable and long-term manufacturing partnership between both parties. The inclusion of a profit-sharing mechanism further aligns interests, fostering continued cooperation in optimizing yield, performance, and market reach. According to Frost & Sullivan, it is an industry norm for DRAM chip design companies and DRAM wafer foundries to enter into agreements similar to the Development Agreement and for the DRAM chip design companies to charge non-recurring engineering fees under such agreements.

Furthermore, in collaboration with globally renowned academic institutions, multiple research papers co-authored by our team have been accepted at premier international conferences, including IEEE S&P, one of the top four conferences in computer security, and ACM/IEEE ISCA, a leading academic conference in computer architecture. These achievements underscore our commitment to advancing innovation and contributing to the global technology landscape.

In addition, we partnered with each of (i) Enrigin, which is a leading AI computing chip company, (ii) a high-performance heterogeneous AI computing chip innovator in China and (iii) a premier CPU developer in China, to jointly develop next-generation high-bandwidth memory products during the Track Record Period. These collaborations leverage our partners' cutting-edge chip architecture and our advanced memory design capabilities to deliver optimized performance for data-intensive AI and high-performance computing applications.

INTELLECTUAL PROPERTY

We use various product designs, technologies and know-how that were developed by us or third parties through licensing arrangements. However, we do not rely on any critical intellectual property that is licensed from third parties. We strictly adhere to and implement the relevant laws and regulations concerning patents, trademarks, copyrights, integrated circuit layouts, trade secrets, and other intellectual property, protecting our technologies by registering various types of intellectual property rights or entering into confidentiality agreements. Additionally, we proactively secure patents in advance for high-bandwidth memory and stacking technology to establish a distinct and defensible patent portfolio.

As of the Latest Practicable Date, we had 92 patents, comprising 83 in the PRC, 6 in Japan and 3 in the U.S., 33 trademarks including 25 in the PRC, four in Hong Kong, one in Macau, one in Taiwan and two in Japan, 10 copyrights in the PRC including seven software copyrights, and 11 layout designs of integrated circuit. The table below sets forth the key IP rights and their respective technological significance to us. For details of our intellectual property rights, see the paragraph headed "Statutory and General Information — B. Further Information about our Business — 2. Intellectual property rights" in Appendix V of this document.

Our Product or Technology	Key IP	Patent Number	Application Scenario	Key Functions of Our Product or Technology
8Gb DDR4	3D Stacked Memory Architecture and Its Processing Method, Memory (三維堆疊存儲器架構及其處理方法、存儲器)	202311772980.2	Enterprise-level servers and data centers, PC	DRAM chip
25nm 1Gb DDR3	Storage Array and Method for Improving Data Read Accuracy of Storage Array (存儲陣列及提高存儲陣列的數據讀取準確度的方法)	202410224395.7	(1) Consumer electronics including set-top boxes and printers; (2) network communication equipment	DRAM chip
	A Control Device for Sensing Amplifier Supply Voltage (一種感測放大器供電電壓的控制裝置)	202420751162.8	(1) Consumer electronics including set-top boxes and printers; (2) network communication equipment	DRAM chip
25nm 2Gb DDR3	A Device and Method for Saving Energy During Memory Refresh (一種在存儲器刷新過程中節省能耗的裝置及方法)	202410438368.X	(1) Consumer electronics including set-top boxes and printers; (2) network communication equipment	DRAM chip
	Random Number Generation Method, Device, Electronic Equipment, and Storage Medium (隨機數生成方法、裝置、電子設備和存儲介質)	202411005607.9	(1) Consumer electronics including set-top boxes and printers; (2) network communication equipment	DRAM chip
High-bandwidth memory	Internal Voltage Testing System and Method for Memory (存儲器內部電壓測試系統和方法)	202410526909.4	AI chips, high-performance computing, data centers, graphics processing, autonomous driving	High-bandwidth memory chip
	Memory Redundant Word Line Refresh Method, Device, Equipment, and Medium (存儲器冗餘字線刷新方法、裝置、設備和介質)	202410627719.1	AI chips, high-performance computing, data centers, graphics processing, autonomous driving	High-bandwidth memory chip

Our Product or Technology	Key IP	Patent Number	Application Scenario	Key Functions of Our Product or Technology
8 Gb DDR4 Logic Process Product Design	Fuse Unit for Storage Array and Its Processing Method, Storage Array (用於存儲陣列的熔斷器單元及其處理方法、存儲陣列)	202310824954.3	Enterprise-level servers and data centers, smart home appliances	DRAM chip
	A Clock Correction Circuit and Memory (一種時鐘校正電路和存儲器)	202311006147.7	Enterprise-level servers and data centers, smart home appliances	DRAM chip
	Memory Testing Method, System, and Computer-Readable Storage Medium (內存測試方法、系統及計算機可讀存儲介質)	202211625081.5	Enterprise-level servers and data centers, PC	DRAM module
	A Memory Automation Testing Method and System Based on Hybrid Cloud (一種基於混合雲的內存自動化測試方法和系統)	202211665140.1	Enterprise-level servers and data centers, PC	DRAM module
DDR4 PHY Logic Interface Development	Duty Cycle Detection Method for Delay-Locked Loop Clock Signals and Duty Cycle Detector (延遲鎖相環路時鐘信號佔空比檢測方法、佔空比檢測器)	202310392614.8	Enterprise-level servers and data centers, smart home appliances	DRAM chip

OUR EMPLOYEES

As of December 31, 2025, we had a total of 161 employees. The following table sets forth the number of our full-time employees by function as of December 31, 2025, respectively:

	As of December 31, 2025
	Number of Employees
Function	
R&D	86
Sales and Marketing	26
Administration	21
Operating and Quality Control	19
Senior Management	9
Total	**161**

As of December 31, 2025, 90.7% of our employees were based in the PRC, while the other 9.3% of our employees were based in Japan. To streamline human resource management, we established a comprehensive set of internal management measures, outlining the procedures and criteria for recruitment, training, internal referrals, among others.

We use various recruitment methods, including campus recruitment, online recruitment, other external recruitment channels as well as internal referrals and transfers. In addition to salaries and benefits, we generally offer our full-time employees an annual performance-based bonus tied to our Company's operational results. We have established a comprehensive system for employee training and development, including general trainings on company information and corporate culture, product knowledge, employee rights and responsibilities, workplace safety, data security and other vocational aspects, as well as specific trainings that improve employee knowledge and expertise in certain important areas related to our business. We are committed to making continual efforts to provide an engaging working environment for our employees.

We enter into standard labor contracts and confidentiality agreements with our full-time employees, and we enter into non-competition agreements with our key management and professionals. As required under PRC laws and regulations, we participate in various employee social security plans that are organized by applicable local municipal and provincial governments, including housing, pension, medical, work-related injury, maternity and unemployment benefit plans. We believe we maintain a good working relationship with our employees, and we have not experienced any material labor dispute or any difficulty in recruiting staff for our operations during the Track Record Period and up to the Latest Practicable Date.

INSURANCE

During the Track Record Period, we provided mandatory social insurance for our employees as required by PRC social insurance regulations, such as pension insurance, unemployment insurance, work injury insurance, maternity insurance and medical insurance. We believe that our insurance coverage is in line with the industry practice and adequate to cover our key assets, facilities and liabilities, including but not limited to property all risks insurance, supplementary commercial insurance for employees (including supplementary medical insurance and accidental injury/death insurance), etc. Our Directors consider our insurance policy as a whole to be in line with the general market practice. See "Risk Factors — Risks Relating to Our Industry and Business — We may not have sufficient insurance coverage to cover our potential liability or losses and as a result, our business, financial conditions, results of operations and prospects may be adversely affected should any such liability or losses arise."

QUALITY CONTROL

We emphasize quality control in all aspects of our operations, including product development, component sourcing, product assembly and delivery. We apply strict quality control standards and have implemented various quality control checks to ensure that our products meet our customers' expectations and international and industry standards. We also require our business partners, including wafer manufacturer, packaging and testing service providers, assembly service providers, components suppliers and delivery service companies, to apply their stringent quality control standards and meet our internal requirements. The following outlines the quality control measures at each stage of the production process that we or our production partners have in place:

Procurement of raw materials. We have always been selective in choosing our suppliers for raw materials. We only purchase from qualified suppliers, and the qualification process includes rigorous requirements regarding quality control. See "Production and Procurement — Procurement of Raw Materials, Components and Parts" for detailed supplier selection criteria. We constantly monitor the raw materials we source, and conduct quarterly reviews and evaluations on our suppliers' performance, covering the quality of the components supplied, the timeliness of delivery, pricing and ability to provide value-added services. Pursuant to our arrangement with various suppliers, any components delivered that fail our quality inspection will be returned to our suppliers at their cost, and we will terminate our relationship with such suppliers if they fail to rectify the defects.

Wafer fabrication. During the Track Record Period, we cooperate exclusively with PSMC for wafer fabrication as wafer fabrication requires highly advanced technologies and PSMC is a global leader in wafer fabrication. We understand PSMC, as a leading wafer manufacturer, has stringent quality standards that safeguard the quality of wafers we use for our chips. We inspect wafers before delivery for packaging and testing.

Packaging and testing. Our packaging and testing partners also conduct inspection of the wafers for us. Upon delivery of packaged and tested chips, we further conduct our own inspection to ensure the chips' quality.

Assembly. We have adopted stringent safety and quality standards for final product assembly in addition to those of our third-party subcontractors for assembly services. Specifically, we conduct quality sampling tests on the components used in the assembly process, semi-finished products and final products. We have received ISO9001:2015 certification. We also have a dedicated quality control team responsible for carrying out the quality control procedures based on the ISO9001:2015 standards. We have devoted and will continue to devote significant resources to product quality control. During the Track record Period and as of the Latest Practicable Date, we have not experienced any material product quality disputes.

WARRANTY AND AFTER-SALES SERVICES

We generally provide a warranty period of one year to three years for our products. We maintain timely communication with our customers, promptly address their feedback, and deliver efficient after-sales services. We believe that the provision of satisfactory after-sales services is a crucial determinant of our success. We receive customer feedback through our website, telephone, email and via our extensive network of distributors. We have established an efficient customer complaint handling mechanism, featuring clear responsibilities, rapid root cause analysis, and tiered annual case reviews to drive continuous improvement. These standardized procedures ensure timely responses and effective corrective actions across departments. We provide product return and exchange services that are tailored to address the requirements and concerns of our customer. We developed a standard product return procedure which is detailed in our customer return management policy. When a customer raises a quality issue with our products, we will promptly verify the concern. Following an internal analysis and review that confirms a product deficiency, our quality control department will inform the customer service team to initiate a return request to complete the return and exchange procedure. During the Track Record Period, we did not experience material product returns from our direct sales customers or distributors. In isolated cases, we may coordinate product exchanges for customers to accommodate their adjustments in product designs, product processes and product promotion and marketing arrangements. During the Track Record Period, the amount of such product exchanges was insignificant.

ENVIRONMENTAL, SOCIAL AND GOVERNANCE

Environmental, Social, and Governance Matters

We are keenly aware of the importance of Environmental, Social and Governance (ESG) to sustainable development. Upon [**REDACTED**], we commit to complying with the *Environmental, Social and Governance Reporting Guide* as set out in Appendix C2 to the Rules Governing the Listing of Securities on The Stock Exchange of Hong Kong Limited. On an annual basis, we will publish ESG reports to disclose our ESG performance to stakeholders.

ESG Governance

We have established a top-down, three-tiered ESG governance structure with a clear definition of the responsibilities for ESG matters at each level to ensure the orderly implementation of ESG-related work. The Board of Directors, as the highest decision-making body for ESG governance, is responsible for reviewing ESG objectives, overseeing ESG risks, formulating strategies, and supervising ESG matters. The Audit Committee, operating under the Board of Directors, is responsible for assisting the Board in ensuring the effective implementation of ESG-related work, managing the achievement of ESG objectives, and reporting regularly to the Board on ESG progress. The ESG Working Group, composed of heads of major departments within our Company, is responsible for the day-to-day execution of ESG matters, including ESG risk identification and assessment, ESG information disclosure, ESG performance management, ESG training, and other related activities.

Tackling Climate Change

Climate Change Risks and Opportunities

We recognize that climate change poses long-term impacts on our business operations. We have identified and assessed climate-related risks, taking into account policies and regulations, market concerns, and current climate conditions and trends. The main risks involved include:

- *Physical risks:* Climate change and extreme weather events may directly impact our daily operations. These risks include acute risks (typhoons, floods, heavy rainfalls, and other extreme weather events) and chronic risks (such as long-term changes in climate patterns or sea level rise). We have formulated the *Emergency Response Management Procedures*, which clearly defines the handling processes and personnel responsibilities for responding to potential natural disasters such as typhoons and floods, and also continuously optimized the procedure. We provide allowances for employees working in high temperatures and implement flexible work arrangements to ensure the safety of our employees, customers, and company assets.

- *Transition risks:* In the process of transitioning to a low-carbon economy, we may face risks related to policy, technology, market, and reputation. We continuously monitor the requirements of external policies and laws and stakeholder needs. In addition, we encourage employees to choose low-carbon travel options to ensure the reduction of carbon emissions during our operations. At the same time, we require our suppliers and production partners to take energy-saving and carbon-reducing measures, and actively explore sustainable operating practices across the entire value chain.

Despite facing the aforementioned climate change-related physical and transition risks, we have identified potential business opportunities presented by climate change.

- *Opportunities for industry development:* Memory chips are widely used in key areas of the digital economy, such as smart terminals and data centers, enabling us to capitalize on the development opportunities presented by industrial digitalization and the green and low-carbon transition.

- *Opportunities for technological innovation:* We continuously invest in R&D and improve product energy efficiency performance through technological innovations such as advanced process optimization and low-power design.

- *Opportunities for market demand:* The market demand for green and low-carbon memory products is on the rise. Our products have obtained multiple internationally recognized authoritative certifications, thus meeting the demand of global customers for high-performance, low-power memory solutions.

Energy Management

We strictly adhere to laws and regulations such as the *Law of the People's Republic of China on Conserving Energy*. We have also established energy management systems, including the *Environmental Aspect Inspection and Control Procedures*. Through lean management and energy-saving measures, we continuously strengthen energy consumption management in various operational scenarios and business stages to achieve our energy-saving goals. Specific measures include:

- Encouraging employees to save electricity and energy through internal promotion (such as emails and posters)
- Setting air conditioning temperatures appropriately to ensure efficient energy usage
- Ensuring that devices such as computers, printers, and copiers automatically enter sleep or standby mode when not in use
- Purchasing energy-efficient equipment to reduce unnecessary energy consumption.
- Promoting remote work to lower the energy demand of office spaces

From the initial construction stage of the Jinhua Testing Laboratory, we integrated the concept of energy conservation. The laboratory is equipped with energy-efficient lighting fixtures and a variable-frequency air conditioning control system. Once the testing environment reaches the required constant temperature and humidity, the air conditioning system automatically switches to a minimum power mode to reduce energy consumption. In terms of equipment procurement, we prioritize testing equipment with high energy efficiency ratios. In addition, we established comprehensive equipment usage regulations for the laboratory, explicitly requiring that equipment be operated on an as-needed basis and that main system power be turned off outside of working hours to minimize power loss. We also conduct regular energy audits to identify major energy-consuming items and enhance management of these areas. To foster a culture of collective participation in energy-saving practices, the laboratory organizes annual training and promotional activities focused on energy conservation.

Metrics and Targets

Throughout our operations, we continuously monitor energy usage and performance metrics and also regularly conduct statistical analysis of energy consumption. The data on energy consumption and carbon emissions for the years ended December 31, 2023, 2024 and 2025 are as follows:

Energy Consumption	Unit	2023	2024	2025
Natural gas	m^3	1,521	1,820	2,670
Direct energy consumption	MWh	15.03	17.98	26.38
Direct energy consumption intensity	MWh/RMB million	0.03	0.03	0.01
Purchased electricity*	MWh	654.57	1,002.45	1,679.80
Indirect energy consumption	MWh	654.57	1,002.45	1,679.80
Indirect energy consumption intensity	MWh/RMB million	1.12	1.55	0.02
Total energy consumption	MWh	669.60	1,020.43	1,706.18
Energy consumption intensity	MWh/RMB million	1.15	1.58	0.02

* The increase in purchased electricity during the Track Record Period is primarily attributed to the commissioning of our testing facility located in Jinhua, Zhejiang, as well as the expansion of overall production capacity.

GHG Emissions	Unit	2023	2024	2025
Direct GHG emissions (Scope 1)	tCO_2e	3.29	3.94	5.77
Indirect GHG emissions (Scope 2)	tCO_2e	373.30	571.70	957.99
Total GHG emissions (Scope 1 & 2)	tCO_2e	376.59	575.64	963.76
GHG emission intensity (Scope 1 & 2)	tCO_2e/RMB million	0.65	0.89	0.87
Other indirect GHG emissions in the value chain (Scope 3)	tCO_2e	16,711.17	19,443.32	34,369.74
GHG emission intensity (Scope 1, 2 & 3)	tCO_2e/RMB million	29.44	30.97	31.98

Notes:

(1) The greenhouse gas (GHG) emissions metrics are calculated in accordance with internationally recognized standards and guidelines, including *Greenhouse Gas Protocol* (GHG Protocol) issued by the World Resources Institute (WRI) and the World Business Council for Sustainable Development (WBCSD), the *China Products Carbon Footprint Factors Database (2022)*, the EPA Supply Chain GHG Emission Factors v1.2 (NAICS, CO_2e, USD2021), and the *2021 UK Government GHG Conversion Factors for Company Reporting*.

(2) The energy consumption metrics are calculated in accordance with the national standards of the People's Republic of China, including the *General Rules for Calculation of the Comprehensive Energy Consumption* (GB2589-2020) and the *Guideline of the Greenhouse Gas Emissions Accounting and Reporting – Power Generation Facilities*.

(3) Indirect energy mainly includes purchased electricity.

(4) Direct energy mainly includes natural gas used at our operational sites.

(5) Other indirect GHG emissions in the value chain mainly come from purchased goods and services, capital goods, upstream transportation and distribution, business travel, and employee commuting.

In 2022, we launched the Jinhua Testing Laboratory construction project. From 2023 to 2024, we procured a substantial amount of testing and auxiliary equipment. The laboratory began operations in 2023, with testing capacity gradually expanding. The construction of fixed assets and the acquisition and use of laboratory equipment have been the main drivers of increased energy consumption and carbon emissions over the past two years. Meanwhile, the rapid expansion of the Company's scale has not been immediately accompanied by a corresponding increase in new product sales, resulting in a slight rise in energy consumption and carbon emissions per unit of revenue. To effectively manage and control energy consumption and carbon emissions, we actively taken steps to expand product sales in order to ensure a continuous reduction in both energy consumption and carbon emission intensity.

Moreover, all of our products are manufactured by OEM suppliers, making the purchased goods and services category the primary source of our Scope 3 GHG emissions, accounting for over 90%. In light of this, we have set clear carbon footprint requirements for the products supplied by our OEM partners, aiming to drive more effective energy-saving and carbon-reducing measures during chip manufacturing processes. Through these initiatives, we aim to work collaboratively with stakeholders across the value chain to promote green mobility and further reduce Scope 3 GHG emissions.

In order to effectively track energy consumption and carbon emissions, we have set the following targets. By 2030, we aim to reduce our comprehensive energy consumption intensity and operational carbon emission intensity (Scope 1 & 2) by 15% compared to 2024 levels. Furthermore, we are committed to achieving a year-on-year reduction in our Scope 3 carbon emission intensity.

The specific targets and timeline for energy consumption and carbon emission intensity reduction are as follows:

2024	2025	2026	2027	2028	2029	2030
Baseline year	Drop	3%	6%	9%	12%	15%

Environmental Protection

Adhering to the philosophy of green, eco-friendly sustainable development, the Company is dedicated to minimizing the environmental impact of its business operations. We strictly comply with the *Environmental Protection Law of the People's Republic of China*, the *Law of the People's Republic of China on the Prevention and Control of Environmental Pollution by Solid Waste*, and other applicable laws and regulations. We have established a series of internal environmental management systems, including the *Environmental Aspect Inspection and Control Procedures*, and required all departments and subsidiaries to strictly adhere to these regulations. We have obtained the ISO 14001:2004 Environmental Management System certification.

Water Resource Management

We place high importance on the comprehensive utilization and rigorous management of water resources during the operational process. We implement water-saving measures throughout our business operations and adopt targeted optimization strategies to enhance the efficiency of domestic and laboratory water usage. Specific measures include raising water-saving awareness among employees through emails and posters; reducing water usage in pantry areas by adopting centralized cleaning methods and installing sensor-activated faucets and other water-saving facilities.

We have implemented the following targeted measures:

- Recycling of air conditioning cooling water through a closed-loop circulation system to reduce demand for fresh water;
- Installation of intelligent remote control systems at the equipment end, enabling automatic shutdown of the water supply when the cooling water pressure reaches a predefined standard and the equipment is in standby mode, thereby further increasing water resource efficiency.

Through these measures, we are committed to minimizing water consumption while ensuring the smooth operation of the laboratory, thereby contributing to its sustainable development.

Water Consumption	Unit	2023	2024	2025
Water consumption volume*	Tonne	3,337	5,918	11,290
Water consumption intensity	Tonne/RMB million	5.75	9.16	10.22

* The increase in water usage during the Track Record Period is primarily attributed to the commissioning of our testing facility located in Jinhua, Zhejiang, as well as the expansion of overall production capacity.

As part of our efforts toward water conservation, we have set water-saving targets: by 2030, our water consumption intensity will decrease by 2% annually compared to the previous year.

The specific targets and timeline for water consumption intensity reduction are as follows:

	2024	2025	2026	2027	2028	2029	2030
Baseline year		2%	2%	2%	2%	2%	2%

Emissions Management

As a fabless chip design company, we do not own any manufacturing facilities or vehicles. Therefore, our daily operations do not generate waste gases or wastewater. In terms of waste management, our waste primarily consists of general solid waste generated in offices, warehouses, and laboratories, as well as scrapped chips resulting from testing processes.

We strictly comply with the *Law of the People's Republic of China on the Prevention and Control of Environmental Pollution by Solid Waste* and other relevant laws, regulations, and industry standards. We have formulated the *Waste Management Procedures* to ensure the effective disposal of waste. All waste generated is collected in a centralized manner and transported off-site for disposal in accordance with regulatory requirements. Furthermore, we actively raise employees' awareness of waste reduction and resource efficiency through means such as emails and posters. The main measures include reducing the use of disposable items and encouraging green procurement.

The data on waste emissions and disposal for the years ended December 31, 2023, 2024 and 2025 is as follows:

Waste Emissions	Unit	2023	2024	2025
Total waste emissions*	Tonne	0.36	0.29	0.41
Waste emission intensity	Tonne/RMB million	0.00062	0.00045	0.00037
Proportion of hazardous waste receiving compliant treatment*	%	100	100	100

* Hazardous waste refers to scrapped chips generated during the testing process, 100% of which is crushed and recycled.

Product Responsibility

We strictly adhere to the laws and regulations of the regions where it operates, including the *Product Quality Law of the People's Republic of China* and the *Standardization Law of the People's Republic of China*. We have put in place a comprehensive control plan during the entire process from raw material quality, production and processing testing to packaging and shipment. Each stage is operated and inspected in line with the requirements of the control plan.

Production Process Quality Control Procedures

Besides engaging in product innovation, we have formulated the *Intellectual Property Management Measures* and the *Patent Incentive Management Measures* to emphasize the protection of intellectual property rights and encourage the output of innovative achievements.

Customer Responsibility

Upholding a customer-centric philosophy, we have formulated the *Guidelines on Customer Complaint Handling Operations* to optimize the customer service experience to the greatest extent possible and continually enhance customer satisfaction. We have established a prompt and effective complaint-handling mechanism, held major departments accountable for customer complaints, and set requirements such as the efficiency of response to customer demands. In addition, we have prepared the *Nonconforming Product Quality Control Operation Procedures* to clarify management processes such as product after-sales service and product recall, and continuously optimize our products.

In strict accordance with the *Civil Code of the People's Republic of China* and the *Personal Information Protection Law of the People's Republic of China*, we rigorously protect customer privacy. We have prepared the *Information Security Guidelines* to standardize the management of customer personal information files and continuously optimize our privacy protection system. As of December 31, 2025, we had not experienced any incidents of infringing customer privacy rights or leaking customer information.

Employee Management

We strictly comply with relevant laws and regulations such as the *Labor Law of the People's Republic of China* and the *Labor Contract Law of the People's Republic of China*. The specific guidelines for compliant recruitment have been outlined in the *Employee Handbook*. We explicitly prohibit any form of child labor or forced labor, and ensure that our recruitment processes are fair and impartial.

In addition, we provide our employees with competitive compensation and a wide range of benefits, including but not limited to festival allowances, supplementary commercial insurance, paid annual leave, health check-ups, employee training and development programs, and high-temperature subsidies. These measures aim to fully safeguard employees' rights and interests, enhance job satisfaction, and support employees in achieving a healthy work-life balance.

We have developed scientific training programs for all employees. Through standardized and systematic training management, we enhance employees' professional skills and robust human resource support for our Company's growth. Every year, we formulate an *Annual Training Plan* based on business needs.

We strictly comply with laws and regulations such as the *Work Safety Law of the People's Republic of China*, the *Fire Protection Law of the People's Republic of China*, and the *Law of the People's Republic of China on Prevention and Control of Occupational Diseases*. We arrange annual health check-ups for all employees and provides necessary labor protection articles for factory and warehouse staff to safeguard their health. As of December 31, 2025, we had not experienced any incidents of work-related injury or death.

Anti-corruption

We adhere strictly to laws and regulations such as the *Anti-Unfair Competition Law of the People's Republic of China* and the *Anti-Monopoly Law of the People's Republic of China*. We have formulated the *Regulations on Anti-Commercial Bribery Management System* to maintain a sound business ethics environment. We have set up an Integrity Leading Group, whose members include our general manager, chief financial officer, head of audit, and head of legal affairs. We have opened a dedicated email account to ensure that key management personnel stay updated on audit developments and promptly address any breaches of business ethics. Meanwhile, we publicly disclose our whistleblowing channels. The Integrity Leading Group conducts internal investigations into the reports and also leverages the expertise of external auditors and lawyers when necessary.

In order to standardize employee conduct, we have detailed the specific requirements of anti-commercial bribery in the *Employee Handbook*. By means of official announcements, we clearly convey our anti-bribery policies and guidelines to all employees in an authoritative manner. Moreover, we incorporate anti-commercial bribery clauses into the new employee onboarding training courses to ensure that every employee acquires an awareness of compliance. As set out in cooperation agreements with customers and suppliers, we explicitly require them to adhere to our anti-bribery terms and uphold the principles of integrity cooperation, thus preventing misconduct at the source of business relationships. As of December 31, 2025, we had not experienced any litigation cases related to violations of business ethics.

RISK MANAGEMENT AND INTERNAL CONTROL

We adopted and continually improve our internal control mechanisms to ensure the compliance of our business operations. Furthermore, we conduct periodic review of the implementation of our risk management policies and internal control measures to ensure their effectiveness and sufficiency.

We are dedicated to upholding the legal compliance of our operations and management, safeguarding assets and ensuring the accuracy and completeness of financial reports and related information. We established an internal audit department tasked with independent audit supervision of the business operations and internal control of our Company in accordance with laws, rules and regulations and Articles of Association, and in accordance with the principles of objectivity, impartiality and prevention.

Our Board is collectively responsible for establishing and implementing such risk management mechanisms and overseeing our overall risk management. Our Directors are of the view that our current internal control measures are adequate and effective.

Compliance Risk Management

Compliance risk refers to the risk of being subject to legal and regulatory sanctions, and the risk of major financial and reputational losses as a result of our failure to comply with relevant laws, regulations, rules and guidelines.

In accordance with such procedures, our operations department conducts supplier selection and evaluation before entering into any contracts or business arrangements, which includes reviewing the suppliers' business qualifications, service history, and key achievements. In addition, our legal department reviews the contract terms and examines related documents, including all necessary due diligence materials and licenses and permits obtained by the other party to fulfill its obligations under the relevant contract.

In addition, we continually monitor changes in relevant laws and regulations as well as the regulatory environment to ensure compliance in our business operations. We delegate the responsibility of monitoring compliance in specific business areas to representatives from those areas. In addition, we have a dedicated department that continuously supervises compliance efforts within departments and reports to our general manager. We also have a department that regularly evaluates and supervises our compliance efforts and reports to our general manager and the Board.

Intellectual Property Risk Management

As a knowledge- and technology-intensive company, we have been and may continue to be subject to claims from companies holding patents or other intellectual property rights, alleging infringement of such rights or otherwise asserting their rights and urging us to obtain licenses in the course of our operations. See "Risk Factors — Risks Relating to Our Industry and Business — Our business may be adversely affected by inadequate protection of intellectual property rights and/or claims by third parties for possible infringement of their rights." To ensure proper management of

our intellectual property and avoid litigation concerning intellectual property infringement, we have implemented various internal policies and established an internal intellectual property management system: (1) we have developed and enacted robust internal policies for the management of intellectual property rights; (2) to facilitate effective management of our intellectual properties, we utilize an internal intellectual property management system for the full lifecycle management of our proprietary intellectual property; (3) to safeguard against potential infringements on both our intellectual property rights and those of others, our legal department, responsible for intellectual property management, conducts thorough searches and analysis of our R&D outcomes upon the completion of scientific research projects and technology development; (4) we require employees to adhere to confidentiality obligations for technical secrets, sign confidentiality contracts and non-compete agreements, and follow an internal confidentiality system outlining specific employee responsibilities; and (5) to foster employees' enthusiasm for research and enhance the protection of our technologies, we have established a patent reward management policy to encourage protecting job-related inventions through patents.

Information Security and Data Privacy Risk Management

See "Data Security and Privacy" in this document.

Anti-corruption Risk Management

Anti-corruption risk refers to the risk of use of cheating, bribery or other illegal measures for (i) the pursuit of improper personal benefits at the expense of our Company's economic interests and (ii) the pursuit of improper interests of our Company. We have established our anti-corruption risk management policies prohibiting any corruption activities by our employees, either for the pursuit of improper personal benefits or improper interests of our Company. We have maintained a whistleblower mechanism for employees to anonymously report any incidents of bribery and corruption. Our internal audit department bears sole accountability for the audit and anti-corruption endeavors of our Company and provides regular reports to the Audit Committee of the Board. We will impose corresponding administrative disciplinary sanctions on persons responsible for corruption incidents. Suppliers, distributors and customers found to engage in corruption incidents shall receive formal warnings, face restrictions on supply or sales, and, where deemed necessary, be placed on a prohibited list. We provide internal training to our employees and ensure that our stakeholders, including customers, distributors, suppliers and shareholders, are informed of our anti-corruption policies and practices.

Audit Committee Experience and Qualification and Board Oversight

To monitor the ongoing implementation of our risk management policies, we have established an Audit Committee to review and supervise our financial reporting process and internal control system on an ongoing basis to ensure that our internal control system is effective in identifying, managing and mitigating risks involved in our business operations. See "Directors and Senior Management — Board of Directors."

In addition to our internal control department, we have also established an internal audit department which is responsible for reviewing the effectiveness of internal controls and reporting issues identified and improving our internal control system and procedures by identifying internal control failures and weaknesses on an ongoing basis. The internal audit department reports any major issues identified to the Audit Committee and Board on a timely basis.

INFORMATION TECHNOLOGY SYSTEMS

IT is fundamental to our competitive edge and operational efficiency. We utilize and maintain IT systems that evolve in tandem with our business growth, ensuring they meet our varied operational demands. These systems underpin key areas such as sales, R&D, supply chain management, production and after-sales services. Our main information technology systems include the following:

- *BI system*: Our business intelligence ("**BI**") system facilitates data integration and analysis to support management decision-making. By collecting and processing operational data from various departments, including inventory, sales, and finance, the system provides real-time business insights and reports. Through data visualization, trend analysis, and predictive models, it helps optimize supply chain management, production planning, and resource allocation.

- *OA system*: Our Office Automation ("**OA**") system integrates functions such as scheduling, document management, workflow, and collaboration to enhance internal efficiency. At the same time, the system provides document management and data analytics features, ensuring document security and assisting our management in optimizing operations.

- *ERP system*: Our Enterprise Resource Planning ("**ERP**") system is designed to integrate various aspects of our business, including finance, procurement, production, logistics, sales, and quality control. It promotes communication and coordination across different departments, thereby improving efficiency and enhancing productivity.

During the Track Record Period and up to the Latest Practicable Date, we had not experienced any material IT system failure or downtime that had a material adverse effect on our business operations. See "Risk Factors — Risks Relating to Doing Business in the Markets in which We Operate — Cybersecurity breaches and other disruptions could compromise our confidential and proprietary information, which could cause our business and reputation to suffer."

DATA SECURITY AND PRIVACY

In recent years, data privacy and cybersecurity have emerged as critical governance priorities for companies worldwide. This is particularly pertinent as the PRC legislature and government authorities regularly introduce new cybersecurity, data security and privacy laws and regulations. Consequently, our practices regarding the collection, use, storage, disclosure and transfer of various types of data may come under increased administrative scrutiny. See "Risk Factors — Risks Relating to Doing Business in the Markets in which We Operate — Cyber security breaches and other disruptions could compromise our confidential and proprietary information, which could cause our business and reputation to suffer" and "Risk Factors — Risks Relating to Our Industry and Business — Any failure to obtain requisite approvals, licenses or permits applicable to our business operation may have an adverse impact on our business, financial condition and results of operations."

In the course of our business operations, we collect, store and process business data and transaction data. Given that we only make transactions with enterprises, our business generally does not involve the collection or processing of customers' personal information.

To reinforce our data security and protection measures, we established comprehensive internal policies. These policies facilitate our data management and provide detailed requirements in relation to the classification, storage, access, transmission, encryption and disposal of data. We closely monitor data security threats and promptly strengthen protective measures to prevent data breaches and system disruptions from impacting our operations and reputation. We also stay vigilant

about changes in data privacy regulations across different countries to ensure compliance and mitigate legal and financial risks. Additionally, we closely follow market regulatory requirements to obtain necessary permits and licenses in a timely manner, preventing potential business disruptions.

Moreover, we implemented a robust information backup management system, which sets forth the guiding principles, detailed procedures and mechanisms for data recovery. In addition, we formulated a manual on information security management to set out the general guidance and principles of our information security management, under which we established a series of policies and procedures, including among others, policies on system operation management, password management and corporate trade secret protection and procedures on document control and confidentiality management. These systems, policies and procedures collectively form a solid framework that safeguards our data and upholds our stringent standards for information security.

COMPETITION

We primarily compete against global and local DRAM chip design companies adopting similar fabless model as ours. According to Frost & Sullivan, DRAM chips are among the most widely used and standardized foundational products in the integrated circuit industry, with market demand showing considerable growth. Based on different product specifications and applications, DRAM can be divided into mainstream DRAM and niche DRAM and our Company specializes in the niche DRAM market. According to Frost & Sullivan, the global niche DRAM market was RMB68.6 billion in 2025. The China (including Hong Kong, Macau and Taiwan) niche DRAM market reached RMB41.6 billion in 2025, and in the next five years, benefiting from the withdrawal of overseas large manufacturers, the technological rise of local manufacturers, as well as the promotion of the Internet of Things and domestic substitution policies, the China (including Hong Kong, Macau and Taiwan) niche DRAM market size is expected to reach RMB95.7 billion by 2030, with a CAGR of 18.2% from 2025 to 2030. See "Industry Overview — Overview of the Global and China Dram Market — Market Drivers and Trends of DRAM Industry — Increase of domestic self-sufficiency rate" in this document.

The principal competitive factors in our markets include technological expertise and innovative R&D capabilities, product development capabilities and supply chain partnerships. We have significant in-house capabilities across critical areas of DRAM chip design and testing and are increasing spending in R&D in key areas, with a focus on the development of AI memory-computing solutions. We offer a comprehensive range of DRAM products to meet diverse customer needs in various segments such as consumer-grade and industrial-grade markets, with wide product applications across consumer electronics, network communications, automotive electronics, energy and industrial control systems. We continue to enhance our existing product portfolio, including the continuous iteration of our DRAM chip offerings, as well as the development of high-bandwidth memory products, focusing on the implementation of 3D heterogeneous integration solutions. In terms of supply chain partnerships, we have established strong, long-term relationships with fabrication foundries and packaging and testing service providers which will further consolidate our competitiveness.

We have demonstrated strong market competitiveness among Chinese companies in the global niche DRAM market. According to Frost & Sullivan, in terms of niche DRAM revenue in 2025, we ranked fifth among Chinese companies and fourth among Chinese fabless companies in the global niche DRAM market. We have developed expertise in Wafer-on-Wafer 3D heterogeneous integration technology and are actively advancing toward achieving mass production of high-bandwidth memory products.

OUR PROPERTIES

Jinhua Property

During the Track Record Period, we entered into a purchase agreement (the "**Purchase Agreement**") with Zhejiang Jinyi Zhiyuan Industrial Co., Ltd.* (浙江金義智園實業有限公司) ("**Jinyi Zhiyuan**") for the acquisition of a testing facility in Jinhua, Zhejiang, with a total gross floor area of 8,286.8 sq.m. ("**Jinhua Property**"). As of the Latest Practicable Date, Jinyi Zhiyuan had obtained the real property ownership certificate of Jinhua Property. We have paid the purchase price for Jinhua Property in full according to the Purchase Agreement and occupied Jinhua Property. As of the Latest Practicable Date, Jinyi Zhiyuan had not completed the registration of the change in right holder for real property ownership certificate, as Jinyi Zhiyuan is currently undergoing internal procedures.

We have obtained a written confirmation from Jinyi Zhiyuan in May 2025 (the "**Confirmation**"), confirming, among others, that: (1) as of the date of the Confirmation, Jinhua Property is free from any mortgage, or other encumbrances, and is not subject to any disputes over debts and claims, or any property preservation measures in litigation, and that there are no defects or other inherent faults that would affect the use of Jinhua Property; (2) we have full rights to own and use Jinhua Property; (3) completing the registration of the change in right holder for real property ownership certificate of Jinhua Property is not subject to any material legal impediments; and (4) we and Jinyi Zhiyuan have no existing or potential disputes, controversies, or claims with respect to Jinhua Property. In addition, Jinyi Zhiyuan undertakes to complete the registration of the change in right holder for real property ownership certificate as soon as possible. As advised by our PRC Legal Advisor, the Purchase Agreement is legally binding on Jinyi Zhiyuan and us. Accordingly, we are entitled to require Jinyi Zhiyuan to complete the registration of the change in right holder for real property ownership certificate of Jinhua Property.

Leased Properties

As of the Latest Practicable Date, we leased (i) six properties in the PRC with an aggregate gross floor area of approximately 2,896 sq.m.; (ii) one property in Hong Kong with a gross floor area of approximately 923 sq.ft.; and (iii) three properties in Japan with an aggregate gross floor area of approximately 249.8 sq.m., all from Independent Third Parties. Our lease agreements in respect of the abovementioned leased properties generally have lease terms ranging from one year to three years. The properties we owned or leased are primarily used for office purposes.

As of the Latest Practicable Date, three of our lease agreements in the PRC were not registered with the relevant competent authorities. We have taken proactive steps to register these lease agreements. As the registration of a lease agreement requires the cooperation between the lessor and lessee, and lessors are typically unwilling to undertake the administrative burden, we were not able to complete the registration of the remaining lease agreements. Pursuant to the applicable laws and regulations in China, property lease agreements for leased properties must be registered with the relevant real estate administration bureaus in China. As advised by our PRC Legal Advisor, the lack of registration does not affect the validity and enforceability of the lease agreements, but we may be subject to fines from RMB1,000 to RMB10,000 for each such lease agreement for failure to register. Our PRC Legal Advisor advises that, if the lease registration can be completed in accordance with relevant laws and regulations within the prescribed time limit ordered by the competent governmental authorities, the risk of governmental authorities imposing a material penalty on us with respect to these leased properties is remote. During the Track Record Period and up to the Latest Practicable Date, we had not been subject to any material penalties arising from the non-registration of our lease agreements, and had not experienced any dispute arising out of, or in relation to, our leased properties.

In addition, the lessor of one of our leased properties with an aggregate gross floor area of 1,689.6 sq.m. was unable to provide a valid title certificate as of the Latest Practicable Date. As advised by our PRC Legal Advisor, it is the landlord's responsibility to obtain a title certificate, and, we, as the lessee, will not be subject to any material penalties. We may not be able to continue to use such property if the validity of such lease is challenged by third parties, in which case we will have to relocate to other premises. Since the leased property is primarily used as our office space and is substitutable, such relocation may involve additional costs but would not have a material adverse impact on our business operation. As of the Latest Practicable Date, we were not aware of any challenge by third parties or government authority of such title defect. We cannot assure you that in the future, we may not encounter such challenges. In addition, in the event of relocation, the additional costs could adversely affect our daily operation and cause an impact on our financial condition.

As of the Latest Practicable Date, we had no owned property interest that forms part of our non-property activities that has a carrying amount of 15% or more of total assets pursuant to Rule 5.01(2)(b) of the Listing Rules.

AWARDS AND RECOGNITIONS

During the Track Record Period, we have received awards and recognitions, including, but are not limited to, the following:

Award/Recognition	Award Year	Awarding Institutional/Authority
National-Level Specialized and Sophisticated Key "Little Giant" Enterprise (國家級專精特新重點「小巨人」企業)	2025	The Ministry of Industry and Information Technology of the PRC
National Specialized and New "Little Giant" Enterprise (國家級專精特新"小巨人"企業)	2024	The Ministry of Industry and Information Technology of the PRC
Provincial Enterprise Research and Development Institution (省級企業研發機構)	2024	Zhejiang Provincial Department of Economy and Information Technology
Most Innovative and Dynamic Small and Medium Enterprise (最具創新活力中小企業獎)	2024	Zhejiang Semiconductor Industry Association
"Gold Member"	2024	Diversity Computing Promotion Committee of the China Communications Standards Association
Global Computing Alliance Membership Certificate (全球計算聯盟會員證書)	2024	Global Computing Alliance
Member of the China Automotive Chip Industry Innovation Strategic Alliance (中國汽車芯片產業創新戰略聯盟會員)	2024	China Automotive Chip Industry Innovation Strategic Alliance
Zhejiang Province Specialized and New Small and Medium-sized Enterprises (浙江省專精特新中小企業)	2023	Zhejiang Provincial Department of Economy and Information Technology

LICENSES, APPROVALS AND PERMITS

We are subject to laws, regulations, and supervision by different levels of regulatory authorities and are required to maintain various licenses, permits and certificates in order to conduct our business. A summary of such relevant laws and regulations which our business operations are subject to is set out in the section headed "Regulatory Overview" in this document.

During the Track Record Period and up to the Latest Practicable Date, we had obtained all the material requisite licenses, qualifications and permits from the relevant regulatory authorities, and all of our material licenses, qualifications and permits were valid and subsisting as of the Latest Practicable Date. There were no certificates that are expired or not yet renewed as of the Latest Practicable Date. Our Directors are of the view that there are no material legal impediments in renewing the licenses that will be expiring.

LEGAL AND REGULATORY COMPLIANCE

Legal Proceedings

We may from time to time become a party to various legal or administrative proceedings arising in the ordinary course of our business. Litigation or any other legal or administrative proceeding, regardless of the outcome, is likely to result in substantial cost and diversion of our resources, including our management's time and attention. For more information, please see "Risk Factors — Risks Relating to Our Business and Industry — We are subject to risks relating to litigations and disputes with employees, competitors, business partners or other parties, which could adversely affect our business, financial condition, results of operations and prospects." in this document.

During the Track Record Period and up to the Latest Practicable Date, there had been no legal proceedings pending or threatened against us or our Directors that could, individually or in the aggregate, have a material adverse effect on business, financial condition and results of operations.

Compliance

During the Track Record Period and up to the Latest Practicable Date, we had not been and were not involved in any material non-compliance incidents that have led to fines, enforcement actions or other penalties that could, individually or in the aggregate, have a material adverse effect on business, financial condition and results of operations.

BUSINESS ACTIVITIES IN RELATION TO REGION AND ENTITY SUBJECT TO INTERNATIONAL SANCTIONS AND ENTITY SUBJECT TO EXPORT CONTROLS

During the Track Record Period, the Group has sold certain self-developed smart memory chips, wafers to non-sanctioned customers based in the Relevant Region. The Group has engaged certain Taiwan-based non-sanctioned foundry and packaging firms to manufacture certain items which are classified as EAR99. Most of the items that fall within the scope of the EAR but are not specifically controlled for export, are given the classification of EAR99. EAR99 items generally consist of low-technology consumer goods and do not require a license in most situations. As advised by our International Sanctions Legal Advisers after performing the procedures they consider necessary, the Group's activities with the Relevant Region and its procurement of EAR99 items did not implicate the applicable U.S. Export Controls or represent a Primary Sanctioned Activity on the basis that i) we are not a Sanctioned Target; ii) the Relevant Region is not subject to a general and comprehensive export, import, financial or investment embargo under sanctions related law or regulation of the Relevant Jurisdiction; and iii) our customers based in the Relevant Regions are not sanctioned, thus our procurement and corresponding sales of such items in the Relevant Regions did not represent a violation to the export controls applicable such items.

During the Track Record Period, the Group has also sold certain DRAM module incorporated with DRAM DIE that are non-U.S. origin and are not subject to the EAR to two customers which have been designated by the BIS to the Entity List. The Group has reviewed the compliance of the transactions before proceeding with the in-country transfer to the said Entity List customers, and has received confirmation from our supplier that such DRAM DIE are not subject to the EAR. As advised by our International Sanctions Legal Advisors, based on the information provided by the Group, on the basis that such DRAM DIE are non-U.S. origin and are not subject to the EAR, such export did not implicate the U.S. Export Controls applicable to the said Entity List customers, and hence did not represent a Primary Sanctioned Activity or a violation of the U.S. Export Controls.

As advised by our International Sanctions Legal Advisors, on the basis that we did not engage in any activities targeted by extra-territorial provisions of sanctions law or regulation in the Relevant Jurisdictions, the prohibitions and wider restrictions under EU, UK and UK Overseas Territories sanctions measures as applicable during the Track Record Period, are not implicated by the Group's business activities in the Relevant Region.

IMPACT OF U.S. OUTBOUND INVESTMENT RESTRICTIONS

The Outbound Investment Rule

On October 28, 2024, the U.S. government issued the Provisions Pertaining to U.S. Investments in Certain National Security Technologies and Products in Countries of Concern (the "**Outbound Investment Rule**"). The Outbound Investment Rule implements Executive Order 14105, dated August 9, 2023, entitled "Addressing United States Investments in Certain National Security Technologies and Products in Countries of Concern." The rules impose investment prohibition and notification requirements on U.S. persons for a wide range of investments in entities associated with China (including Hong Kong and Macau) that are engaged in activities relating to: (i) semiconductors and microelectronics, (ii) quantum information technologies, and (iii) artificial intelligence systems, collectively defined as "covered foreign persons." Unless an exception applies, U.S. persons subject to the Outbound Investment Rule are prohibited from making, or required to report, certain investments in covered foreign persons, which are defined as "covered transactions." The "covered transactions" include acquisitions of equity interests that are not yet publicly traded, certain debt financing, joint ventures, and certain investments as a limited partner in a non-U.S. person pooled investment fund.

The Outbound Investment Rule excepts from its coverage (among other transactions) investments in "publicly traded securities" as defined in the Outbound Investment Rule — i.e., denominated in any currency that trade on a securities exchange or over-the-counter in any jurisdiction. Notably, this exception does not apply to investments that afford a U.S. person rights beyond "standard minority shareholder protections," as defined in the Outbound Investment Rule, with respect to the covered foreign person.

The Outbound Investment Rule took effect on January 2, 2025, and applies to transactions with a completion date on or after that date. Notably, on February 21, 2025, the America First Investment Policy Memorandum was issued aiming to potentially further expand the set of technologies and targeted investment types.

Impact of the Outbound Investment Rule on our Group

Our legal advisor as to the Outbound Investment Rule and our Directors are of the view, and the Sole Sponsor concurs, that the impact of the Outbound Investment Rule is generally limited and manageable because:

- Investments by persons other than U.S. persons or their "controlled foreign entities," as defined under the Outbound Investment Rule, are generally not subject to the Outbound Investment Rule, unless a U.S. person is involved in a manner that constitutes "knowingly directing" a "prohibited transaction" by a non-U.S. person.

- We are likely a "covered foreign person," and our business likely constitutes "covered activities" under the Outbound Investment Rule. As a result, investments by U.S. persons in us could constitute "notifiable transactions" under the Outbound Investment Rule. An exception to the notifiable transaction regime applies to investments by U.S. persons in publicly traded securities, including securities traded on a non-U.S. exchange such as the Stock Exchange, as long as the trade does not afford a U.S. person rights beyond standard minority shareholder protections with respect to the covered foreign person. Where this exception applies, the transaction is an excepted transaction and is not subject to notification.

- According to guidance published by the U.S. Department of the Treasury in December 2025, absent additional facts, a U.S. person's acquisition of an equity interest pursuant to a subscription agreement or similar arrangement (including a standby [**REDACTED**]) qualifies as an excepted transaction where, at the time of acquisition, the equity interest constitutes a "publicly traded security" within the meaning of the Outbound Investment Rule, regardless of when the relevant agreement was entered into. Neither the Outbound Investment Rule or U.S. Department of the Treasury guidance define the exact time of acquisition. A conservative approach would therefore be to assume that the acquisition of the Company's shares by an investor occurs upon settlement, since an investor would receive the Company's shares at settlement.

- As long as the settlement of the H shares purchased by U.S. persons occurs after 9:00 am on the [**REDACTED**], the H shares they acquire would be publicly [**REDACTED**] and traded securities. However, if settlement occurs before 9:00 am on the [**REDACTED**] when the H shares are not yet publicly [**REDACTED**] and traded (for example, this is the case for settlement for [**REDACTED**]), it remains uncertain whether the publicly traded securities exception under the Outbound Investment Rule can be applicable. As a result, the Outbound Investment Rule may increase the compliance burden on U.S. investors who wish to invest in us during the [**REDACTED**].

- While there is no assurance that the U.S. Department of the Treasury will take the same view, it is the responsibility of the U.S. person engaged in a "notifiable transaction" to make the relevant notification. Therefore, the Outbound Investment Rule is not expected to have a material adverse impact on our business, results of operations, financial condition or the [**REDACTED**].

- The U.S. government may enact future regulations altering the current regime. On December 18, 2025, the U.S. Congress enacted the Comprehensive Outbound Investment National Security Act of 2025 ("**COINS Act**") as part of the National Defense Authorization Act for Fiscal Year 2026, which codifies and expands the Outbound Investment Rule and provides independent statutory authority for the program for at least seven years. The COINS Act directs the Treasury to expand and clarify the scope of "excepted transactions" within 450 days of enacting the COINS Act, including preserving the publicly traded securities exception, and adding a new exception for certain secondary transactions, including underwriting services that include the temporary acquisition of an equity interest.

TRANSFER PRICING ARRANGEMENTS

During the Track Record Period, our Company and Zentel Japan had been engaged in certain material intra-group transactions (the "**Relevant Transactions**") involving the buy-sell transactions of DRAM chips. The major types of our intra-group transactions include the procurement by Zentel Japan of DRAM chips from our Company for reselling to certain overseas customers during the Track Record Period.

The Organization for Economic Co-operation and Development ("**OECD**"), an international organization fostering cross-border cooperation, issued the Transfer Pricing Guidelines for Multinational Enterprises and Tax Administrations (the "**OECD Transfer Pricing Guidelines**"). These guidelines are widely adopted by tax authorities worldwide in evaluating related-party transactions. In accordance with the OECD Transfer Pricing Guidelines, transactions within our Group's entities should be carried out in commensurate with the arm's length principle.

We have engaged independent third party tax advisers to provide analysis on the Relevant Transactions. Based on the independent third party tax adviser's assessment of the Relevant Transactions and the transfer pricing benchmarking analysis, which involved screening and evaluating comparable companies, the profitability of the relevant entities could be considered as reasonable and commensurate with their respective functions and risks. Therefore, no significant transfer pricing risk was identified in the Relevant Transactions for the years ended December 31, 2023, 2024 and 2025.

Our Directors confirm that during the Track Record Period and up to the Latest Practicable Date, we were not aware of any enquiries, audit, investigation or challenge by any tax authorities in the PRC and other relevant tax jurisdictions in relation to our intra-group transactions and transfer pricing arrangements. Our Directors believe that our intra-group transactions were in line with the arm's length principle and we were in compliance with the relevant transfer pricing laws and regulations during the Track Record Period and up to the Latest Practicable Date.

IMPACT OF COVID-19

The outbreak of COVID-19 pandemic has adversely affected the global economy since the first quarter of 2020. Numerous anti-pandemic measures were taken by government authorities, including travel bans and restrictions, quarantines measures and remote working arrangements. The adverse impact of the pandemic has gradually subsided since 2023.

The impact of the COVID-19 pandemic on our overall business operations was limited and did not have any material impact on our Group's operation and financial condition. During the Track Record Period and up to the Latest Practicable Date, we did not experience any material disruption to our regular operations, raw material procurement or product delivery due to the COVID-19 pandemic. In response to the pandemic, we implemented various measures in line with government policies and regulations to ensure the maintenance of stable operations. Accordingly, our Directors believe that the pandemic has not had any material adverse impact on our business operations and financial performance during the Track Record Period.

BUSINESS SUSTAINABILITY AND PATH TO PROFITABILITY

Business sustainability

We have experienced a continuous improvement in the sales of our major products during the Track Record Period, demonstrating our ability to successfully commercialize our products and solutions. During the Track Record Period, the total storage capacity of our products sold grew from approximately 29.3 million GB in 2023 to approximately 54.3 million GB in 2025, representing a CAGR of 36.1%. Accordingly, our revenue increased from RMB580.3 million in 2023 to RMB1,104.9 million in 2025. According to Frost & Sullivan, in terms of niche DRAM revenue in 2025, we ranked fifth among Chinese companies and fourth among Chinese fabless companies in the global niche DRAM market. The global and China (including Hong Kong, Macau and Taiwan) DRAM, in particular, high-bandwidth stacked DRAM, markets are expected to continue with expansion, which will ensure the demand for our DRAM products and AI memory-computing solutions in the coming years. According to Frost & Sullivan, the global market for high-bandwidth stacked DRAM products reached RMB217.6 billion in 2025, with a further CAGR of 26.2% predicted from 2025 to 2030. With further penetration and development of our DRAM products and AI memory-computing solutions, we expect that our revenue from such products and solutions will continue to gain momentum and improve our financial condition in the foreseeable future.

Analysis of historical losses

We incurred loss of RMB244.3 million, RMB108.9 million and RMB10.5 million for the three years ended December 31, 2025. Our net loss in 2023 was primarily attributable to the substantial share-based payment expenses incurred during the year. Our adjusted net loss (non-IFRS measure) in the years ended December 31, 2024 was RMB93.2 million and RMB52.8 million, respectively. We had adjusted net profit (non-IFRS measure) of RMB26.1 million for the year ended December 31, 2025. We did not achieve a net profit during the Track Record Period, primarily due to the following factors:

(a) *Prioritization of business expansion over short-term profitability*: During the Track Record Period, we prioritized the development and continuous expansion of our DRAM products in the niche market, which we believe to have high market growth potential. According to Frost & Sullivan, the China (including Hong Kong, Macau and Taiwan) niche DRAM market recorded remarkable growth from 2021 to 2025 and is expected to continue to grow from 2025 to 2030. As the niche DRAM market in China (including Hong Kong, Macau and Taiwan) presents significant market potential, we strategically invested in our business and prioritized the business expansion and market share growth instead of short-term profitability to capture the market opportunities in the rising market. In addition, we have been developing our AI memory-computing solutions, which have not materialized into our revenue but have demonstrated high market potential. According to Frost & Sullivan, driven by the robust demand for AI computing, high-bandwidth stacked DRAM is set to significantly outpace the overall DRAM market, and the high-bandwidth stacked DRAM market can potentially expand at a CAGR of approximately 26.2% from approximately RMB217.6 billion in 2025 to around RMB696.9 billion in 2030, accounting for about 25.9% of the total DRAM market by 2030. In anticipation of the trends of AI computing, we have made significant progress in the R&D of our AI memory-computing solutions and have accumulated valuable technologies and product pipelines. Product design, development, innovation and iteration is often a complex, time consuming and costly process involving significant investment in R&D. For example, our Wafer-on-Wafer 3D heterogeneous integration technology enables direct bonding of logic and DRAM wafers in a vertically stacked configuration, which enhances real-time inference and training performance, making it ideal for data centers, autonomous systems, and other latency-sensitive workloads. Leveraging the accumulation of cutting-edge technologies and industry expertise, we expect to commercialize our first high-bandwidth 3D stacked DRAM chip in 2026. For details of our technologies and products under development in relation to our AI memory-computing solutions, please see "Research and development — Our R&D Capabilities in AI Memory-Computing Solutions" in this section. During the Track Record Period, our R&D expenses amounted to RMB77.2 million, RMB95.8 million and RMB102.1 million respectively, representing 13.3%, 14.8% and 9.2% of our revenue in the respective periods.

(b) *Fluctuations in prices of raw materials for DRAM chips*: During the Track Record Period, the prices of our raw materials, mainly wafers used in the production of DRAM chips, have been subject to significant fluctuations. For the three years ended December 31, 2025, the average unit price of wafers was RMB5,486.2, RMB5,750.0 and RMB5,010.4 per wafer, respectively. These fluctuations have been driven by a combination of the features of the "silicon cycle", supply chain disruptions, changes in global commodity prices, and increased demand. Between 2020 and 2021, supported by the upward trend in the DRAM industry, customer inventory accumulation, and the reduction of DDR3 production capacity by Samsung and SK Hynix, supply-demand imbalances significantly pushed up wafer prices. At the same time, the pandemic caused severe global supply chain constraints, raw material shortages, and logistics disruptions, further tightening supply. In addition, rising global energy and commodity prices increased the cost of silicon materials, leading to a surge in wafer prices. From 2022 to

2024, as end-market demand weakened and inventory levels remained high, the DRAM industry entered a downward cycle, resulting in a sharp decline in demand and a subsequent drop in wafer prices. Against this industry backdrop, the unit price of wafers that we contracted to procure before the market price decline in 2022 but consumed later was relatively high. Such increased cost has had a direct impact on our profitability. In response, we have implemented strategies to mitigate these risks, including maintaining longstanding relationship with key suppliers and exploring alternative materials and processes to reduce our dependence on volatile raw material prices. For example, we maintained long-term partnerships with PSMC, a globally renowned wafer foundry to ensure quality of the wafers. We had entered into production capacity reservation agreement with PSMC where necessary and have established collaborations with ADATA and Ramaxel, two of the world's top 10 DRAM module manufacturers according to Frost & Sullivan, ensuring a stable and robust supply chain. In addition, we dynamically adjusted purchasing volumes based on market price forecasts. When price increases were anticipated, we proactively increased procurement to optimize cost efficiency and reduce exposure to price volatility. While we have been successful in maintaining long-term relationship with our suppliers, we are still subject to the volatility of the market. For example, according to Frost & Sullivan, in 2022, major manufacturers had scaled up DDR3 production. However, growth in end-market demand fell short of expectations. To speed up inventory clearance, companies resorted to price reductions, triggering a decline in DDR3 prices. As a result, the unit price of wafers that we contracted to procure before the market price decline in 2022 but consumed later was relatively high. Such increased cost has had a direct impact on our profitability. During the Track Record Period, our raw material costs amounted to RMB386.8 million, RMB446.6 million and RMB788.5 million, respectively, representing 69.2%, 76.2% and 85.1% of our total costs of sale in the respective years. Since April 2023, monthly meetings have been held to review key business metrics, including sales, pricing trends, inventory turnover, and procurement strategies across product lines, with a focus on aligning procurement with real-time market conditions.

Path to Profitability

We expect to improve our financial performance and achieve profitability in the near future through continual revenue growth, growing economies of scale and improving operating efficiency.

Achieving Sustained Growth in Revenue

We seek to drive continual overall revenue growth through the following measures:

- *Product portfolio expansion and solution customization*: We are expanding and deepening our DRAM product portfolio to address the increasingly diverse requirements of high-growth segments such as AI computing, cloud data centers, and automotive electronics. This includes the development of next-generation low-power and high-bandwidth DRAM solutions, upgrading DDR product technology and developing advanced process product technologies. For example, leveraging the technologies we have accumulated in relation to AI memory-computing solutions, we expect to commercialize the first high-bandwidth 3D stacked DRAM chip in 2026. We also plan to commercialize the first generation of our HSM product by 2026. By closely collaborating with customers in these verticals, we are also offering more application-specific and modular solutions, increasing our value proposition and stickiness.

- *Customer diversification and strategic partnerships*: To mitigate customer concentration risk and tap into new demand pools, we are actively diversifying our customer base. We are also deepening our engagement with our business partners, such as (i) PSMC on advanced wafer processes and (ii) a high-performance heterogeneous AI computing chip innovator in China on 3D stacked and customized high-bandwidth memory, through

strategic alliances and co-innovation initiatives. Specifically, we have entered into a development agreement with PSMC in respect of the development of DRAM products based on 19nm and below nodes, which is a testament of our R&D prowess and our close collaboration with our production partners. These relationships enhance our solution integration capabilities and accelerate our go-to-market execution.

- *Global market penetration and localized customer engagement*: With a solid customer base worldwide, we will deepen collaborations with existing customers while actively pursuing a global strategy. Through our regional R&D and technical support centers in China and Japan, tailored marketing campaigns, and active participation in industry forums, we are gaining actionable market insights. In addition, we plan to strengthen our overseas sales and engineering support teams to improve customer retention. Furthermore, we are committed to integrating global supply chain resources to improve delivery capabilities, enabling faster product launches and quicker responses to international customer demands. These efforts also enhance our responsiveness to regulatory environment changes.

- *Enhancement of industry chain integration capabilities*: We will progressively enhance our industry chain integration capabilities. With the aim to accelerate our high-bandwidth memory strategy through mergers and acquisitions, we will target primarily companies with leading in-memory processing technologies or commercialized applications. In addition, leveraging our testing facility in Jinhua, Zhejiang, we will expand our packaging and testing capacity within the industry chain and explore investments or acquisitions to ensure stable and efficient production.

- *Capturing Market Opportunities*: Although the historical downturn in the niche DRAM market has exerted an adverse impact on our revenue, gross margins and operating cash flow, the recent recoveries, such as the supply-driven price increase in 2025, could potentially boost our revenue, profitability and improve our working capital flexibility. In particular, according to Frost & Sullivan, since the end of 2024, global leading DRAM manufacturers have shifted their business focus toward high-end DRAM products required for the AI market and accelerated their exit from the niche DRAM segment. As the top three global DRAM manufacturers accounted for approximately 70% of the niche DRAM market in 2024, their strategic pivot triggered the supply contraction, subsequently an increase of market price of niche DRAM, according to Frost & Sullivan. This market price increase, if sustained, could assist us in achieving more predictable and sustainable growth.

Narrowing Loss

Historically, our gross margin has been under pressure due to raw material costs and inventory management. Notwithstanding this, our gross margin improved from gross profit margin of 3.7% in 2023 to gross profit margin of 16.1% in 2025. Our efforts to continuously improve margin and achieve long-term profitability include:

- *Volume scaling*: Higher volumes enable better unit economics. We are aligning our go-to-market strategy with volume customers, particularly in fast-growing segments like IoT devices and AI computing, to achieve scale and spread fixed costs more effectively. This effort is supported by our plans to upgrade our production and testing equipment, ensuring stable and efficient production to meet increasing demand. For example, we intend to procure equipment for testing of high-bandwidth memory products, construct our proprietary test production and testing line for DRAM chips and DRAM modules, and enhance our laboratory analytical capability. For details, please see "Future Plans and Use of [**REDACTED**]" in this document. Our Directors believe that we will be able to capture the market demand in the high-bandwidth stacked DRAM market. The domestic AI industry is currently experiencing rapid growth, driving strong demand for

high-bandwidth memory products such as HSM and 3D stacked memory. The Chinese government provides strong support for chip design and the AI sectors. For example, the Interim Measures for the Administration of Generative Artificial Intelligence Services issued in 2023 explicitly encourage independent innovation in key technologies such as AI algorithms, frameworks, and chips, which reflects the Chinese government's strategic emphasis on hardware self-reliance, encouraging greater R&D investment and accelerating breakthroughs in domestic AI chip design and application. Globally, HBM products are mainly supplied by Samsung, SK Hynix, and Micron, with no mainland China company yet commercializing high-bandwidth memory products according to Frost & Sullivan. According to the same source, we are one of the few domestic companies that have developed high-bandwidth 3D stacked memory technology, demonstrated by our (a) independent development of a "1 Logic Wafer + 1 DRAM Wafer" solution, (b) ongoing development of HSM1 product with memory cube commencing tape-out, logic die design completed and certain HSM1-related technology licensed out, (c) commercialization of silicon interposer solutions for advanced packaging, and (d) revenue generated from design services and licensing fees related to our AI memory-computing solutions during the Track Record Period. To capture the growing demand for high-bandwidth stacked DRAM, we plan to focus on the following strategies: (i) advancing our proprietary technologies such as stacked DRAM, HSM1 product and silicon interposer development, while generating revenue through design services and licensing; (ii) upgrading testing capabilities, including building proprietary testing lines and enhancing analytical capacity, to ensure stable and efficient and accurate design and output; and (iii) targeting high-volume customers in fast-growing segments such as AI servers and IoT devices to achieve economies of scale.

- *IP and design reuse*: By reusing proven IP across multiple product lines, we reduce engineering time and lower the risk of design flaws that affect yields and cost. Benefiting from the long-standing R&D experience that we have inherited from Zentel Japan, and our extensive experience and iterative approach in technology development from SDR to DDR4 products, we are able to enhance product performance through design improvements, meet customization needs of our customers through technical adaptation and improve R&D efficiency through technological accumulation. We are also exploring investments or acquisitions in companies with leading in-memory processing technologies to integrate advanced IP and design capabilities into our product development pipeline, further enhancing our ability to reuse and optimize designs. For details, please see "Future Plans and Use of [**REDACTED**]" in this document.

- *Test cost optimization and yield improvement*: Testing is a material contributor to our gross cost. We are utilizing a pre-designed MBIST to reduce time and cost per unit without sacrificing quality. Building on our existing testing facility in Jinhua, Zhejiang, which is dedicated to DRAM chip and module testing, we plan to further strengthen our product testing capabilities to enhance efficiency and reduce overall test costs. For the three years ended December 31, 2025, our Jinhua testing facility was primarily used for internal R&D testing and was not engaged in large-scale commercial testing. As of the Latest Practicable Date, our Jinhua testing facility had a designed daily testing capacity of approximately 80,000 units for DRAM chips and approximately 8,000 units for DRAM modules. Our DRAM IC testing capacity utilization rate was approximately 20%, while our DRAM module testing capacity utilisation rate was approximately 30%, as of the Latest Practicable Date. In addition, we are working closely with foundry partners to improve wafer yields by optimizing our design-for-manufacturing practices. This includes refining layout, reducing process variation sensitivity, and implementing automated design correction tools.

Improving Cash Flow Performance

To improve cash flow, we seek to focus on both operational efficiency and financial discipline:

- *Enhanced inventory management*: Our inventories mainly include raw materials, work in progress and finished products. As of December 31, 2023, 2024 and 2025, we had inventories of RMB158.3 million, RMB152.8 million and RMB299.4 million, respectively. Our business model requires us to manage our inventories efficiently. We will adopt a dynamic, data-driven approach that aligns with the cyclical nature of the DRAM market. Given the volatility in demand and pricing, we will leverage real-time demand forecasting tools and collaborative planning with key customers to enhance accuracy in procurement and production scheduling, preventing both overstocking and shortages. These proactive management approaches enables us to respond more swiftly to market shifts and avoid holding excess inventory during periods of price decline which may lead to impairment. By aligning inventory levels more closely with market trends and actual customer demand, we reduce the likelihood of inventory devaluation due to obsolescence or unfavorable market conditions. In addition, we will seek to diversify supplier relationships to shorten lead times and negotiate flexible payment terms, reducing prepayment burdens. To mitigate obsolescence risks, we will prioritize modular designs that allow for component reuse across product lines and establish inventory hedging strategies to offset price declines.

- *Receivables and payables optimization*: Our trade receivables primarily include amounts due from our customers for products in the ordinary course of business. The credit period granted to our customers was generally one month from the date of billing. Our trade receivables turnover days increased from 46 days in 2023 to 60 days in 2024, as a result of the increase in our trade receivables further due to our business growth in 2024. Our trade receivables turnover days decreased to 44 days in 2025 mainly due to our collection efforts. We plan to achieve our full-year break-even target by clearing long aging inventories and strengthening accounts receivable management. On the payables side, we are also better utilizing the credit periods granted to us to optimize cash flow and preserve liquidity.